# SERVICE MANUAL FOR

## 8889

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MiTAC

# 8889 N/B Maintenance

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# 1. Hardware Engineering Specification

## 1.1 Introduction

### 1.1.1 General Description

This document describes the system hardware engineer specification for 8889 portable notebook computer system.The 8889 notebook computer is a new mainstream high performance thin and light notebook in the MiTAC notebook family.

### 1.1.2 System Overview (1)

Table 1. Hardware Specification

| | |
|---|---|
| CPU | - AMD Mobile K8 (35W/25W) Processers<br>- Athlon64 35W 2700+/2800+/3000+/3200+/3400+<br>- Athlon64 25W 3000+/3200+<br>- AthlonXP-M (32bit) 25W 2500+/2700+ |
| Core logic | - VIA K8N800 North Bridge:with Int.Unichrome Pro VGA SouthBridge:VT8235 |
| L2 Cache | - Lancaster 1MB/ Odessa, Oakville 512 KB/ Dublin 256KB, on CPU die, depends on CPU |
| System BIOS | - Insyde - 512 KB Flash ROM<br>- Includes System BIOS, VGA BIOS, and Plug & Play capability<br>- ACPI 2.; DMI 2.3.1 compliant Boot Sequence (FDD – CDROM – HDD – LAN) |

## 1.1.2 System Overview (2)

Continue to the previous page

| | |
|---|---|
| Memory | - No on Board Memory<br>- Two 200 pin SO DIMM socket for Memory expansion<br>- Support PC-2100/2700/3200 |
| ROM Drive | - 12.7mm Height<br>- 24X CD ROM Drive<br>- 8X DVD ROM Drive<br>- DVD Combo<br>- Combo DVD-RW |
| HDD | - 2.5” 9.5 mm height: 30/40/60/80GB<br>- Support ATA100/133 |
| FDD | - Support External FDD w/z USB 1/F; 3.5 Format for 720KB/1.2MB/1.44MB |
| Display | - 14.1 XGA TFT Display; Resolution:1024x768<br>- 15” XGA TFT Display; Resolution:1024x768 |
| Video Controller | - Int.Unichrome Pro |
| Keyboard | - 19mm key pitch/ 3.0mm key stroke/ 307mm length<br>- Windows Logo Key x 2; Application Key x 1 |
| Pointing Device | - Glide pad with 2x buttons |
| PCMCIA | - 1 Type II slot,Card Bus port support |
| Indictor | - 3 LEDs for Power/Battery charge/WLAN status (on Inverter module)<br>- 5 LEDs for HDD Access,ODD Access, Num lock, Cap lock and Scroll Lock |

## 1.1.2 System Overview (3)

Continue to the previous page

| | |
|---|---|
| Audio System | - Build-in AC-Link Audio controller<br>- AC97 V2.2 Codec<br>- Function key volume control<br>- Built-in Mono Microphone<br>- Speakers x2 ( 1 W in system side )”  with speaker box. |
| I/O Port | - Standard USB2.0 x 4<br>- RJ-11 modem port x 1<br>- RJ-45 LAN port x 1<br>- DC input x 1<br>- VGA out (PC99 Spec)<br>- Microphone jack x 1 (PC99 Spec)<br>- TV-Out (4 pin) x 1 (Resolution up to 1024 x 768)<br>- Line out x1 (PC99 Spec) |
| Communication | - Built-in 56Kbps V.90 modem<br>- Built-in 10/100 M based-T LAN |
| Battery | - 6-cell (Target: 2Hrs Battery Mark for 25WCPU) 2000/2200mAH Li-Ion  Battery support (reserved for 9 Cell Longer Battery Life) |
| AC adapter | - Universal AC adapter 60W (P); Input: 100-240V,50/60Hz AC (support power on charge) |
| Dimensions | - 326x277x22~36.7mm |
| Weight | - 3.0kg |

# 1.2 Hardware System

## 1.2.1 CPU Mobile AMD K8 (Athlon64) Processor

The AMD Athlon™ 64 processor is the most advanced PC processor for mobile computing, providing outstanding performance for demanding software applications. The AMD Athlon 64 processor was also designed to enhance mobility, incorporating AMD PowerNow!™ technology to deliver performance on demand while helping to extend system battery life. The AMD Athlon 64 processor runs on AMD64 technology, and is the first PC processor to run 32-bit applications at full speed while enabling a new generation of powerful 64-bit software applications.

The AMD Athlon 64 processor is designed with your current and future computing needs in mind. Notebook computers with the AMD Athlon 64 processor are able to deliver desktop-class performance for the most demanding software applications. With the AMD Athlon 64 processor, mobile users can enjoy outstanding performance on PC software including productivity, entertainment, and gaming. As the first PC processor for notebook computing to run on the AMD64 platform, the AMD Athlon 64 processor can provide superior performance on today's software with complete readiness for the coming wave of 64-bit computing.

**Compatible with Existing 32-Bit Code Base**

- Including support for SSE,SSE2,MMX™,3DNow!™ technology and legacy x86 instructions.
- Runs existing operating system and drivers
- Local APIC on-chip

**AMD64 Technology**

- AMD64 technology instruction set extensions
- 64-bit integer registers,48-bit virtual addresses,40-bit physical addresses

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- Eight new 64-bit integer registers (16 total)
- Eight new 128-bit SSE/SSE2 registers (16 total)

**64-Kbyte 2-Way Associative ECC-Protected L1 Data Cache**

- Two 64-bit operations per cycle,3-cycle latency

**64-Kbyte 2-Way Associative Parity-Protected L1 Instruction Cache**

- With advanced branch prediction

**16-Way Associative ECC-Protected L2 Cache**

- Exclusive cache architecture — storage in addition to L1 caches
- 1 Mbyte,512-Kbyte and 256-Kbyte options

**Machine Check Architecture**

- Includes hardware scrubbing of major ECC-protected arrays

**Power Management**

- Multiple low-power states
- System Management Mode (SMM)
- ACPI compliant, including support for processor performance states

**Electrical Interfaces**

- HyperTransport™ Technology: LVDS-like differential, unidirectional
- DDR SDRAM: SSTL_2 per JEDEC specification

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- Clock, reset, and test signals also use DDR SDRAM-like electrical specifications

**754 Pin Package Specific Features**

- Packaging
  - 754 pin lidded micro PGA
  - 1.27-mm pin pitch
  - 29x29 row pin array
  - 40mm x 40mm organic substrate
- Integrated Memory Controller
  - Low-latency, high-bandwidth
  - 64-bit DDR SDRAM at 100,133,166, and 200 MHz
  - Supports up to three unbuffered DIMMs
  - ECC checking with double-bit detect and signal-bit correct
- HyperTransport™ Technology to I/O Devices
  - One 16-bit link supporting speeds up to 800 MHz (1600 MT/s) or 3.2 Gigabytes/s in each direction

## 1.2.2 CoreLogic_VIA K8N800 + VT8235CE

### 1.2.2.1 VIA K8N800

**Product Features :**

- **Defines Highly Integrated Solutions for Performance PC Mobile Designs**
  - High performance North Bridge with HyperTransport interface to AMD™ K8 CPU plus AGP 8x external bus to external Graphics Controller plus-speed V-Link interface to South Bridge
  - Combines with VIA VT8235 V-Link South Bridge for integrated LAN, Audio, ATA133IDE and 6 USB 2.0 ports
  - 578 Ball Gird Array package with 35 x35 mm body size and 1.27mm ball pitch
  - 1.5V core, 0.15 u process
- **High Performance Host Interface**
  - Chipset support for AMD™ K8 / ClawHammer™ processor
  - Processor interface via HyperTransport bus
  - Separate “transmit” and “receive” buses for no lost “bus turnaround” cycles
  - All transmit and receive signals use 2 pin low-voltage-swing differential signaling for high-reliability and high speed
  - 8 or 16-bit control / address / data transfer both directions
  - 800 / 600 / 400 / 200 MHz clock rates with “Double Data Rate” –style operation for 1600 / 1200 / 800 / 400 MT/s (Mega-Transfers per second) in both directions simultaneously (total 6.4 GB/sec using 16-bit data transfer mode)

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- Default 8-bit/ 200 MHz operation on startup for high reliability with speedup to dual 16-bit, 800 MHz operation (6.4 GB/sec total bandwidth) under software control (transmit and receive may be different widths and / or speeds)

- **Full Featured Accelerated Graphics Port (AGP) Controller**
  - AGP v3.0 compliant 8x / 4x transfer mode with Fast Write support
  - 1.5V AGP I/O interface
  - Pipelined split-transaction long-burst transfers up to 2.1 GB/sec
  - Supports Side Band Addressing (SBA) mode
  - Supports Flush / Fence commands
  - Supports DBI (Dynamic Bus Inversion)
  - Pseudo-synchronous AGP and CPU interfaces with optimal skew control
  - Thirty-two level read and write request queue
  - One-ninety-two level (quadwords) of write data FIFO
  - Sixty-four level (quadwords) of write data FIFO
  - Graphics Address Relocation Table (GART)
    - One level TLB structure
    - Sixteen entry fully associative page table
    - LRU replacement scheme

- **High Bandwidth 533 MB/Sec 8-Bit V-Link Host Controller**
  - Supports 66 MHz, 4x and 8x transfer modes, V-Link Host interface with total bandwidth of 533 MB/sec

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- Half duplex transfers with separate command / strobe for 4x 8-bit mode, full duplex for 8x 4 bit mode
- Request / Data split transaction
- Transaction assurance for V-Link Host-to-Client access eliminates V-Link Host-Client Retry cycles
- Intelligent V-Link transaction protocol to minimize data wait-state and throttle transfer latency
- Highly efficient V-Link arbitration with minimum overhead

- **Advanced System Power Management Support**
  - ACPI 2.0 and PCI Bus Power Management 1.1 compliant
  - Supports HTSTOP# (HyperTransport Bus Stop) protocol
  - Low-leakage I/O pads

- **Integrated Graphics with 2D /3D / Video Controllers**
  - Optimized Unified Memory Architecture (UMA)
  - Supports 16 / 32 / 64 MB Frame Buffer sizes
  - 200MHz Graphics Engine Clock
  - Internal AGP 8x performance
  - Two independent 128-bit data paths between North Bridge and graphics core to improve video performance, one for frame buffer access and one for texture / command access
  - PCI v2.2 Host Bus compliant
  - AGP v3.0 compliant

- **2D Acceleration Features**

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- 128-bit 2D graphics engine
- Supports ROP3,256 operations
- Supports 8bpp, 15/16 bpp and 32 bpp color depth modes
- BitBLT (Bit Block Transfer) functions including alpha BLTs
- True-color hardware cursor (64x64x32bpp)
- Color expansion, source Color Key and destination Color Key
- Bresenham line drawing / style line function
- Transparency mode
- Window clipping
- Text function

**3D Acceleration Features**

- 3D Graphics Processor
  - 128-bit 3D graphics engine
  - Floating-point setup engine
  - Internal full 32-bit ARGB format for high rendering quality
  - 8K Texture Cache
- Capability
  - Supports ROP2
  - Supports various texture format, including: 16 / 32bbp ARGB, 1 / 2 / 4 / 8bbp Luminance, 1 / 2 /4 / 8bbp Intensity, 1 / 2 / 4 / 8bbp Palletized (ARGB), YUV 422 / 420, and compressed texture (DXTC)

- Texture sizes up to 2048x2048
- Microsoft DirectX texture filter for Nearest, Linear, Bi-linear and Anisotropic modes
- Flat and Gouraud shading
- Vertex Fog and Fog Table
- Z-Bias, LOD-Bias, Polygon offset, Edge Anti-aliasing and Alpha Blending
- Bump mapping and cubic mapping
- Hardware Back-Face culling
- Specular Lighting

- Performance

  - Two texture per pass
  - Triangle rate up to 4.5 million triangles per second
  - Pixel rate up to 200 million pixels per second for 2 textures each
  - Texel bilinear fill rate up to 400million texels per second
  - High quality dithering

**Video Acceleration Features**

- High Quality Video Processor

  - RGB555, RGB565, RGB8888, YUV422 and YUV420 video playback formats
  - High quality 5-tap horizontal and 5-tap vertical (up or down) for both horizontal and vertical scaling (linear interpolation for horizontal and p-scaling and filtering for horizontal and vertical down-scaling)
  - Color and Chroma key support

- Color enhancement for contrast, hue, saturation and brightness
- YUV-to-RGB color space conversion
- Bob and Weave de-interlacing modes
- Tear-free double / triple buffer flipping
- Input video vertical blanking or line interrupt
- Video gamma correction

- Video Overlay
  - Simultaneous graphics and TV video playback overlay
  - Supports video window overlay
  - Supports both YUV and RGB format Chroma key
  - Supports 16 operations for Color and Chroma key
  - Hardware sub-picture blending
- MPEG Video Playback
  - MPEG-2 hardware slice layer, iDCT and motion compensation for full speed playback
  - High quality DVD video playback
  - DVD playback auto-flipping
  - DVD sub-picture playback overlay

**DuoView+™ Capability**

- WinXP, WinME and Win98 multi-monitor, extended desktop support
- Provides two independent display engines, each of which can display completely different information at

different resolutions, pixel depths and refresh rates

- Improved display flexibility with simultaneous FPD /CRT, FPD / TV, FPD / CVI and other combined operations

- **Full Software Support**
  - Microsoft DirectX 7.0, 8.0 and 9.0 compatible
  - Microsoft DirectX Texture Compression (DXTC / S3TC)
  - Support OpenGL™
  - Drivers for majoy operating systems and APIs: Windows® 9x / ME, Windows 2000, Windows XP, Direct3D™, DirectDraw™, DirectShow™ and OpenGL™ ICD for Windows 89x / ME and XP
  - Windows NT 4.0 Standard VGA driver

- **Extensive Display Support for External Video Output**
  - A dedicated CRT display interface
  - A dedicated Digital Video Port supporting TV-Out or TMDS interface
  - An AGP-multiplexed 12-bit interface to external TMDS transmitter for driving a DVI monitor
  - An AGP-multiplexed 24-bit / Dual 12-bit FPD interface to LVDS transmitter

- **CRT Display**
  - CRT display interface with 24-bit true-color RAMDAC up to 300 MHz pixel rate with gamma correction capability
  - Supports CRT resolutions up to 1920x1440

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- **12-bit TMDS Transmitter Interface**
  - 12-bit, 1.5V low-swing, DVD interface for connecting DVI Monitor through TMDS transmitter
  - 12-bit DDR and clock rate up to 165 MHz
  - Built-in digital phase adjuster to fine tune signal timing between clock and data bus
- **TV-Out Interface**
  - 12-bit DVO interface to external TV encoder for ATSC, NTSC or PAL TV display
  - 1.5V signaling on GDVP0 port or 3.3V signaling on DVP0 port
- **24-bit FPD (Flat Panel Display) Interface**
  - 24-bit SDR or DDR mode with LVDS transmitter for 18 / 24-bit interfaced LCD panel
  - Supports panel resolutions up to 1600x1200
- **Dual 12-bit FPD Interface**
  - Dual 12-bit DDR interface with LVDS transmitter for 18 / 24-bit interfaced LCD panel
  - Single or separate sets of clock and sync signals
  - Supports panel resolutions up to 1600x1200
- **Advanced Graphics Power Management Support**
  - Built-in reference voltage generator and monitor sense circuits
  - Automatic panel power sequencing and VESA DPMS (Display Power Management Signaling) CRT power-down

- External I/O signal controls enabling of graphics controller into standby / suspend-off state
- Auto clock gating for inactive functions to achieve maximum power savings
- I²C Serial Bus and DDC / E-DDC Monitor Communications for Plug-and Play configuration

### 1.2.2.2 VT8235 CE

The VT8235 Version CE South Bridge is a high integration, high performance, power-efficient, and high compatibility device that supports Intel and non-Intel based processor to V-Link bus bridge functionality to make a complete Microsoft PC2001-compliant PCI/LPC system. The VT8235 Version CE includes standard intelligent peripheral controllers:

a) IEEE 802.3 compliant 10 / 100 Mbps PCI bus master Ethernet MAC with standard MII interface to external PHYceiver

b) Master mode enhanced IDE controller with dual channel DMA engine and interlaced dual channel commands. Dedicated FIFO coupled with scatter and gather master mode operation allows high performance transfers between PCI and IDE devices. In addition to standard PIO and DMA mode operation, the VT8235 Version CE also supports the UltraDMA-133, 100, 66, and 33 standards to allow reliable data transfer at rates up to 133 MB/sec. The IDE controller is SFF-8038i v1.0 and Microsoft Windows-family compliant.

c) Universal Serial Bus controller that is USB v2.0 / 1.1 and Universal HCI v2.0 / 1.1 compliant. The VT8235 Version CE includes three root hubs with six function ports with integrated physical layer transceivers. The USB controller allows hot plug and play and isochronous peripherals to be inserted into the system with universal driver support. The controller also implements legacy keyboard and mouse support so that legacy software can run transparently in a non-USB-aware operating system environment.

d) Keyboard controller with PS2 mouse support.

e) Real Time Clock with 256 byte extended CMOS. In addition to the standard ISA RTC functionality, the integrated RTC also includes the date alarm, century field, and other enhancements for compatibility with the ACPI standard.

f) Notebook-class power management functionality compliant with ACPI and legacy APM requirements. Multiple sleep states (power-on suspend, suspend-to-DRAM, and suspend-to-Disk) are supported with hardware automatic wake-up. Additional functionality includes event monitoring, CPU clock throttling and stop (Intel processor protocol), PCI bus clock stop control, modular power, clock and leakage control, hardware-based and software-based event handling, general purpose I/O, chip select and external SMI.

g) Full System Management Bus (SMBus) interface.

h) Integrated bus-mastering dual full-duplex direct-sound AC97-link-compatible sound system.

i) Plug and Play controller that allows complete steerability of all PCI interrupts and internal interrupts / DMA channels to any interrupt channel. One additional steerable interrupt channel is provided to allow plug and play and reconfigurability of on-board peripherals for Windows family compliance.

The VT8235 Version CE also enhances the functionality of the standard ISA peripherals. The integrated interrupt controller supports both edge and level triggered interrupts channel by channel. The integrated DMA controller supports type F DMA in addition to standard ISA DMA modes. Compliant with the PCI-2.2 specification, the VT8235 Version CE supports delayed transactions and remote power management so that slower ISA peripherals do not block the traffic of the PCI bus. Special circuitry is built in to allow concurrent operation without causing dead lock even in a PCI-to-PCI bridge environment. The chip also includes eight levels (double words) of line buffers from the PCI bus to the ISA bus to further enhance overall system performance.

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**Product Features :**

- **Inter-operable with VIA Host-to-V-Link Host Controller**
  - Combine with KT400A for a complete DDR Athlon system
  - Combine with CLE266 for a complete DDR VIA C3 / Pentium 3 system
  - Combine with P4X400 for a complete DDR Pentium 4 system
- **High Bandwidth 533 MB/s 8-bit V-Link Client Controller**
  - Supports 66 MHz V-Link Client interface with total bandwidth of 533 MB/sec
  - V-Link operates in 2x, 4x, and 8x modes
  - Full duplex commands with separate Strobe / Command
  - Request / Data split transaction
  - Configurable outstanding transaction queue for V-Link Client accesses
  - Auto Client Retry to eliminate V-Link Host-Client Retry cycles
  - Intelligent V-Link transaction protocol to eliminate data wait-state / throttle transfer latency; all V-Link transactions for both Host and Client have a consistent view of transaction data depth and buffer size to avoid data overflow.
  - Highly efficient V-Link arbitration with minimum overhead; all V-Link transactions have predictable cycle length with known Command / Data duration
  - Auto connect / reconnect capability and dynamic stop for minimum power consumption
  - Parity checking to insure correct data transfers
- **Integrated Peripheral Controllers**

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- Integrated Fast Ethernet Controller with 1 / 10 / 100 Mbit capability
- Integrated USB 2.0 Controller with three root hubs and six function ports
- Dual channel UltraDMA-133 / 100 / 66 / 33 master mode EIDE controller
- AC-link interface for AC-97 audio codec and modem codec
- HSP modem support
- Integrated DirectSound compatible digital audio controller
- LPC interface for Low Pin Count interface to Super-I/O or ROM

**Integrated Legacy Functions**

- Integrated Keyboard Controller with PS2 mouse support
- Integrated DS12885-style Real Time Clock with extended 256 byte COMS RAM and Day/Month Alarm for ACPI
- Integrated DMA, timer, and interrupt controller
- Serial IRQ for docking and non-docking applications
- Fast reset and Gate A20 operation

**Concurrent PCI Bus Controller**

- 33 MHz operation
- Supports up to six PCI masters
- Peer concurrency
- Concurrent multiple PCI master transactions; i.e., allow PCI masters from both PCI buses active at the same time

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- Zero wait state PCI master and slave burst transfer rate
- PCI to system memory data streaming up to 132Mbyte/sec (data sent to north bridge via high speed V-Link Interface)
- PCI master snoop ahead and snoop filtering
- Eight DW of CPU to PCI posted write buffers
- Byte merging in the write buffers to reduce the number of PCI cycles and to create further PCI bursting possibilities
- Enhanced PCI command optimization (MRL, MRM, MWI, etc.)
- Four lines of post write buffers from PCI masters to DRAM
- Sixteen levels (double-words) of prefetch buffers from DRAM for access by PCI masters
- Delay transaction from PCI master accessing DRAM
- Transaction timer for fair arbitration between PCI masters (granularity of two PCI clocks)
- Symmetric arbitration between Host/PCI bus for optimized system performance
- Complete steerable PCI interrupts
- PCI-2.2 compliant, 32 bit 3.3V PCI interface with 5V tolerant inputs

**Fast Ethernet Controller**

- High performance PCI master interface with scatter / gather and bursting capability
- Standard MII interface to external PHYceiver
- 1 / 10 / 100 MHz full and half duplex operation
- Independent 2K byte FIFOs for receive and transmit
- Flexible dynamically loadable EEPROM algorithm

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- Flexible dynamically loadable EEPROM algorithm
- Physical, Broadcast, and Multicast address filtering using hashing function
- Magic packet and wake-on-address filtering
- Software controllable power down

- **UltraDMA-133 / 100 / 66 / 33 Master Mode EIDE Controller**
  - Dual channel master mode hard disk controller supporting four Enhanced IDE devices
  - Transfer rate up to 133MB/sec to cover PIO mode 4, multi-word DMA mode 2 drives, and UltraDMA-133 interface
  - Increased reliability using UltraDMA-133/100/66 transfer protocols
  - Thirty-two levels (doublewords) of prefetch and write buffers
  - Dual DMA engine for concurrent dual channel operation
  - Bus master programming interface for SFF-8038i rev.1.0 and Windows-95 compliant
  - Full scatter gather capability
  - Support ATAPI compliant devices including DVD devices
  - Support PCI native and ATA compatibility modes
  - Complete software driver support

- **Direct Sound Ready AC97 Digital Audio Controller**
  - AC-Link access to 4 CODECs (AC97 + AMC97 + MC97)
  - Multichannel Audio
  - Bus Master Scatter / Gather DMA

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- Dedicated read and write channels supporting simultaneous stereo playback and record
- Dedicated read and write channels supporting simultaneous modem receive and transmit
- 1 stereo DirectSound channel with source / volume control / mixer
- 1 shared FM / SPDIF PCM read channel
- 1 dedicated channel supporting multi-channel audio
- 32-byte line-bufers for each SGD channel
- Programmable 8bit / 16bit mono / stereo PCM data format support
- AC97 2.2 compliant  VT8235 Version CE V-Link South Bridge

- **System Management Bus Interface**

  - Host interface for processor communications
  - Slave interface for external SMBus masters

- **Universal Serial Bus Controller**

  - USB v2.0 and Enhanced Host Controller Interface (EHCI) v1.0 compatible
  - USB v1.1 and Universal Host Controller Interface (UHCI) v1.1 compatible
  - Eighteen level (doublewords) data FIFO with full scatter and gather capability
  - Three root hubs and six function ports
  - Integrated physical layer transceivers with optional over-current detection status on USB inputs
  - Legacy keyboard and PS/2 mouse support

- **Sophisticated PC2001-Compatible Mobile Power Management**

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- Supports both ACPI (Advanced Configuration and Power Interface) and legacy (APM) power management
- ACPI v2.0 Compliant
- APM v1.2 Compliant
- CPU clock throttling and clock stop control for complete ACPI C0 to C3 state support
- PCI bus clock run, Power Management Enable (PME) control, and PCI/CPU clock generator stop control
- Supports multiple system suspend types: power-on suspends with flexible CPU/PCI bus reset options, suspend to DRAM, and suspend to disk (soft-off), all with hardware automatic wake-up
- Multiple suspend power plane controls and suspend status indicators
- One idle timer, one peripheral timer and one general purpose timer, plus 24/32-bit ACPI compliant timer
- Normal, doze, sleep, suspend and conserve modes
- Global and local device power control
- System event monitoring with two event classes
- Primary and secondary interrupt differentiation for individual channels
- Dedicated input pins for power and sleep buttons, external modem ring indicator, and notebook lid open/close for system wake-up
- 32 general purpose input ports and 32 output ports
- Multiple internal and external SMI sources for flexible power management models
- Enhanced integrated real time clock (RTC) with date alarm, month alarm, and century field
- Thermal alarm on external temperature sensing circuit
- I/O pad leakage control

- **Plug and Play Controller**
  - PCI interrupts steerable to any interrupt channel
  - Steerable interrupts for integrated peripheral controllers: USB, floppy, serial, parallel, and audio
  - Microsoft Windows XPTM, Windows NTTM, Windows 2000TM, Windows 98TM and plug and play BIOS compliant
- **Built-in NAND-tree pin scan test capability**
- **0.22um, 2.5V, low power CMOS process**
- **Single chip 27 x 27 mm, 1.0 mm ball pitch, 539 pin BGA**

## 1.2.3 Memory

- Support unbuffer DDR 200/266/333/400MHz SO-DIMM expandable to 1024MB (2 DDR-SODIMM slots)

Table 2. Memory Expansion Capacity

| Slot1 | Slot2 | Total |
|---|---|---|
| 128MB | 0 | 128MB |
| 128MB | 128MB | 256MB |
| 128MB | 256MB | 384MB |
| 128MB | 512MB | 640MB |
| 256MB | 0 | 256MB |
| 256MB | 256MB | 512MB |
| 256MB | 512MB | 768MB |
| 512MB | 0 | 512MB |
| 512MB | 512MB | 1024MB |

## 1.2.4 I/O Ports

- **CRT Ports**

  - Standard VGA compatible port

  - DDC1 and DDC2B compliant

Table 3. CRT Connector

| PIN | SIGNAL | DESCRIPTION |
|---|---|---|
| 1 | RED | Red analog video output |
| 2 | GREEN | Green analog video output |
| 3 | BLUE | Blue analog video output |
| 4 | Monitor Sense | NC |
| 5 | GND | Monitor Sense |
| 6 | GND | Ground |
| 7 | GND | Ground |
| 8 | GND | Ground |
| 9 | VCC | +5VDC |
| 10 | GND | Ground |
| 11 | Monitor Sense | NC |
| 12 | CRT_DDDA | Data from DDC monitor |
| 13 | CRT_HSYNC | Horizontal Sync control |
| 14 | CRT_VSYNC | Vertical Sync control |
| 15 | CRT_DDCK | Clock to DDC monitor |

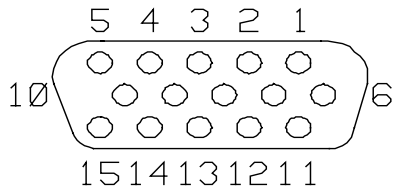



**Figure 1 . CRT Connector**

- **4 Pins S-VIDEO Port for TV-Out**

  - Support up 1024*768 resolution

  - Support PAL and NTSC system.

Table 4. S-Video Port

| Pin | Signal Name | Direction |
|---|---|---|
| 1 | GND | - |
| 2 | GND | - |
| 3 | TV_DACC | O |
| 4 | TV_DACB | O |

## RJ-45

- The Fast Ethernet MAC Controller features an IEEE802.3 and IEEE802.3x compliant MAC with external LAN physical layer chip (VT6103) supporting full duplex 10 Base-T,100 Base-T Ethernet.

- Support Wake-up On-LAN function in System enter to S3.

Table 5. LAN Port

| Pin | Signal Name | Direction | Description |
|---|---|---|---|
| 1 | PJTX+ | Out | Transmit Data Ring |
| 2 | PJTX- | Out | Transmit Data Tip |
| 3 | PJRX+ | IN | Receive Data Ring |
| 4 | PJ45_PJ4 | - | Internal termination resistor |
| 5 | PJ45_PJ4 | - | Internal termination resistor |
| 6 | PJRX- | IN | Receive Data Tip |
| 7 | PJ45_PJ7 | - | Internal termination resistor |
| 8 | PJ45_PJ7 | - | Internal termination resistor |

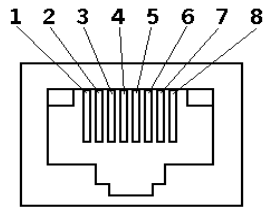



**Figure 2 . LAN Connector**

## RJ-11

- Connection to Modem Daughter Board Connector or Mini-PCI Modem Card.
- Support 56Kbps/V.92 .

Table 6. Modem Port

| Pin | Signal Name | Direction | Description |
|---|---|---|---|
| 1 | NC | - | No Connect |
| 2 | TIP | I/O | Phone Line Positive |
| 3 | RING | I/O | Phone Line Negative |
| 4 | NC | - | No Connect |

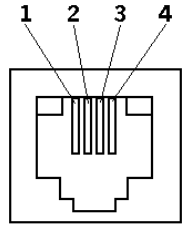



**Figure 3 . Modem Connector**

## USB Ports

- Four industry standard USB 2.0 ports (Backward compatible to USB 1.1)
- Support maximum transfer rate up to 480Mbits/s

Table 7. USB Port

| Pin | Signal Name | Direction | Description |
|---|---|---|---|
| 1 | VCC | Power | USB Device Power (+5VDC) |
| 2 | DATA- | I/O | Balanced Data Negative |
| 3 | DATA+ | I/O | Balanced Data Positive |
| 4 | GND | Power | Ground |

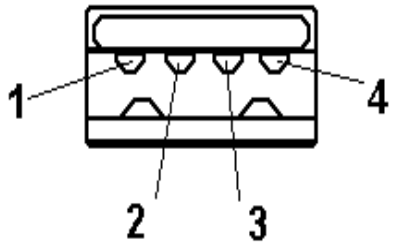



**Figure 4 . USB Connector**

## 1.2.6 PC Card Slot

- One Type II/I slot supporting the 1997 PC Card standard and including full R2 (16-bit) and 32-bit Cardbus data transfer.
- ENE CB714 (PCMCIA Controller) & ENE CP2211 (Power Switch)
- Ability to wake-up from D3-Hot and D3-Cold.
- Mixed-and-match 5V/3.3V 16 bits PC CARDs and 3.3V Cardbus Card.

## 1.2.7 Graphical Subsystem

- Integrated graphics with 2D/3D/Video Controllers
- Support up to 64 MB frame buffer size.
- AGP 8X Interface.

## 1.2.8 Display

- 15”XGA TFT Display; Resolution: 1024x768
- 14”XGA TFT Display; Resolution: 1024x768
- Dual View of LCD+CRT / LCD+TV independent display.
- External Video refresh rate of up to 100Hz supported

  - Vertical refresh frequencies to meet VESA requirements

- Simultaneous video in specified video modes – switchable with hot key

## 1.2.9 IDE Interface

- Support Dual Independent IDE Channels, One is Hard-Disk. The other one is Optical Device.
- Supports PIO mode 0,1,2,3,4,5 and Ultra DMA 33/66/100/133.

## 1.2.10 Read Only Memory (BIOS Flash)

- Fully compatible with industry standard software including Windows XP home & professional edition.
- Fully supports APM V1.2 and latest ACPI specification
- 512Kx8 (4Mbit) Flash BIOS
- Inside BIOS core

## 1.2.11 Power Management Features

- Local standby mode (Individual devices such as HDD, graphics controller, LCD etc..)
- CPU Idle mode (Including ACPI modes C1,C2 and C3)
- Suspend mode (Including S1 and S3 ACPI modes)
- Fully APM V1.2 compliant

- Fully ACPI V1.1 compliant
- Hibernate for Windows XP
- Thermal management
- Fully US EPA Energy Start compliant

## 1.2.12 Keyboard Controller

- Winboard W83L950D

## 1.2.12 LEDs Indiactor

- CDROM & HDD & NUM & CAP & SCROLL & Wireless & 2 LEDs for Power/Battery status Indicator.

## 1.2.13 Touch Pad Module

- Synaptics TM42P-309.

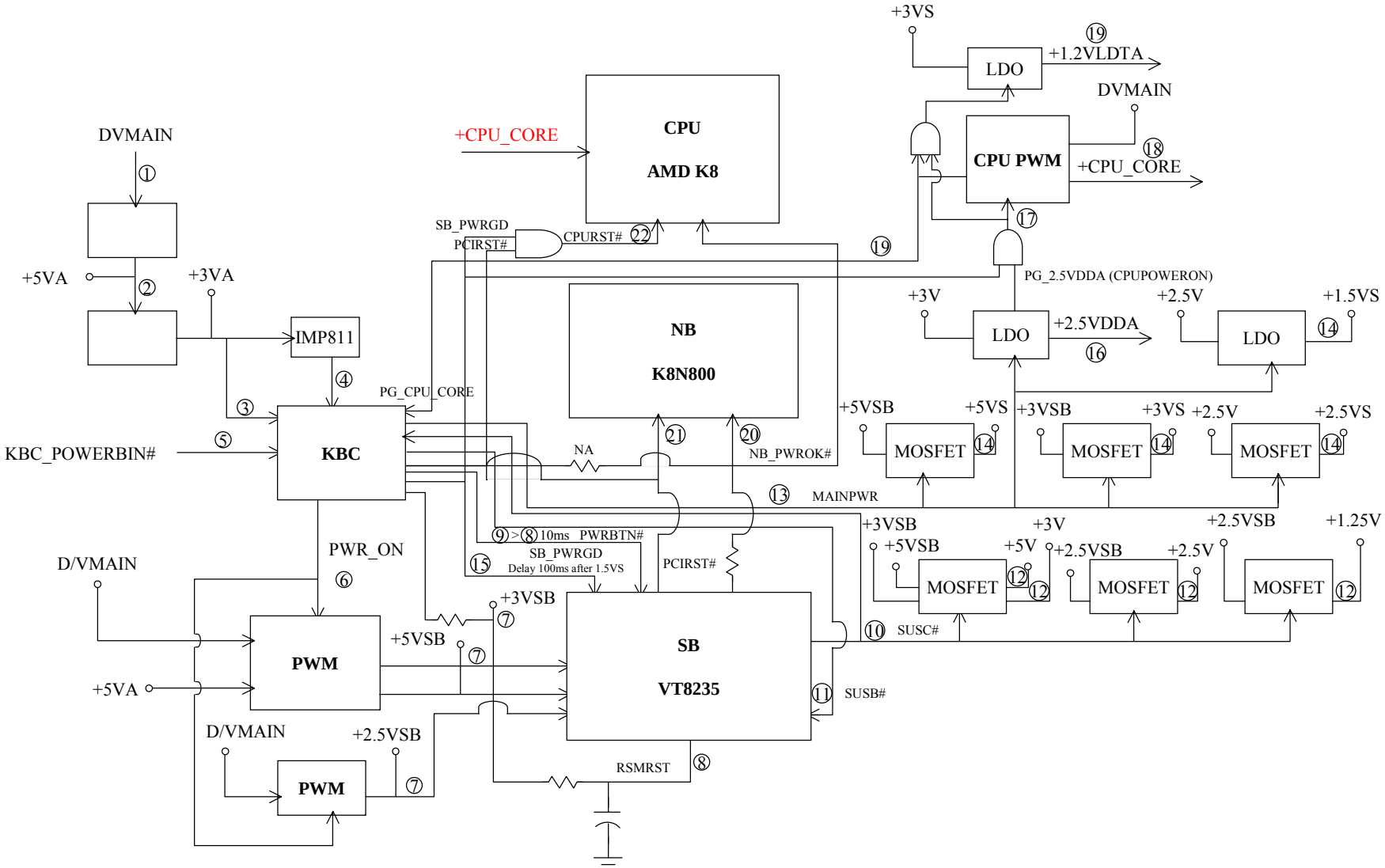
## 1.2.14 Modem (MDC) - Option

Table 8. Modem Daughter Board Connector

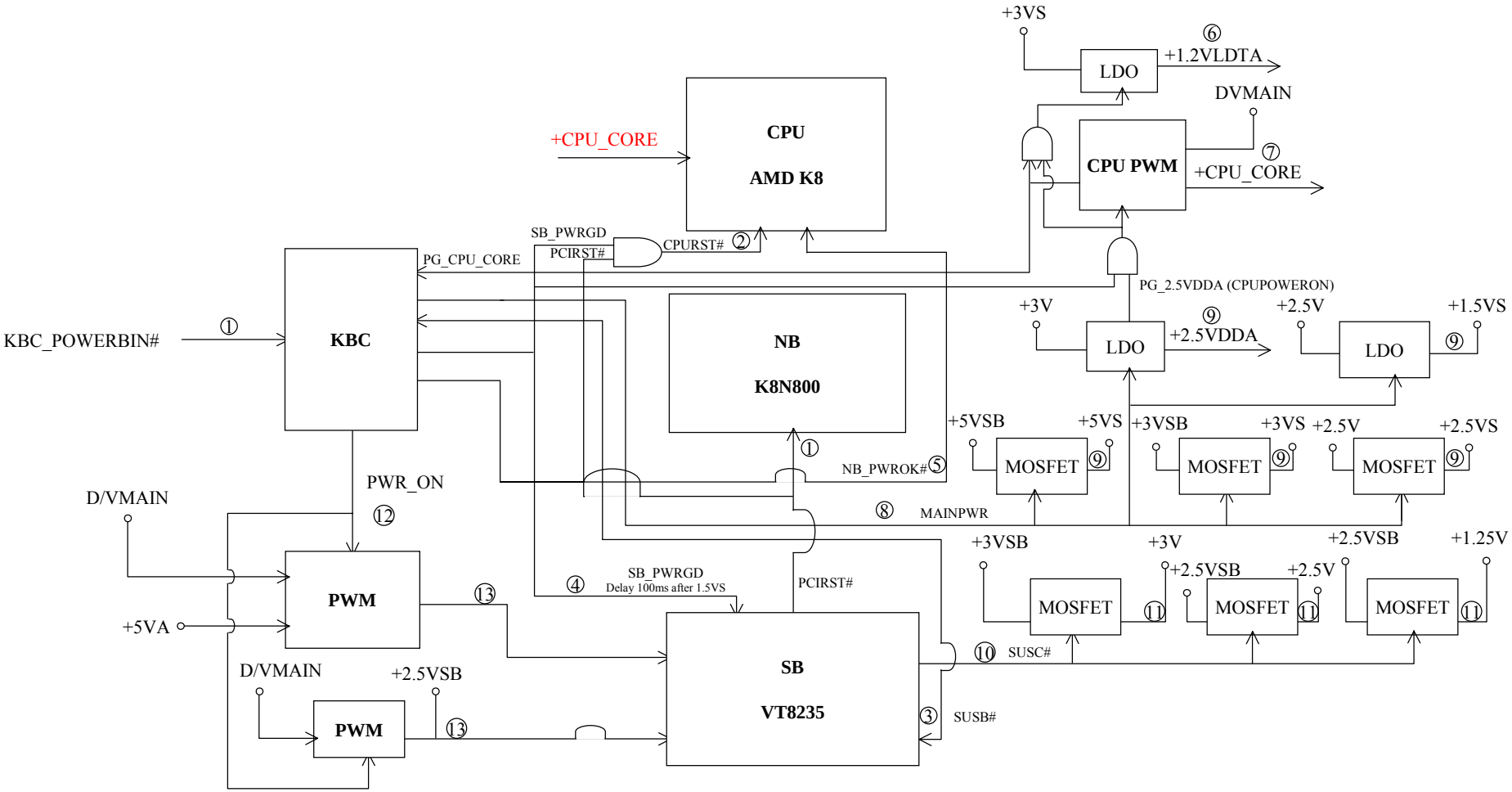
| PIN | SIGNAL NAME | PIN | SIGNAL NAME |
|---|---|---|---|
| 1 | MONO_OUT | 2 | NC |
| 3 | GND | 4 | MODEM_SPK |
| 5 | NC | 6 | NC |
| 7 | NC | 8 | GND |
| 9 | NC | 10 | +5V |
| 11 | NC | 12 | NC |
| 13 | NC | 14 | NC |
| 15 | GND | 16 | Pull Up to +3V |
| 17 | +3V | 18 | +5V |
| 19 | GND | 20 | GND |
| 21 | +3V | 22 | ACSYNC |
| 23 | ACSDOUT | 24 | MSDIN |
| 25 | -ACRST | 26 | MSDIN |
| 27 | GND | 28 | GND |
| 29 | GND | 30 | ACBITCLK |

# 1.3 Electrical Characteristic

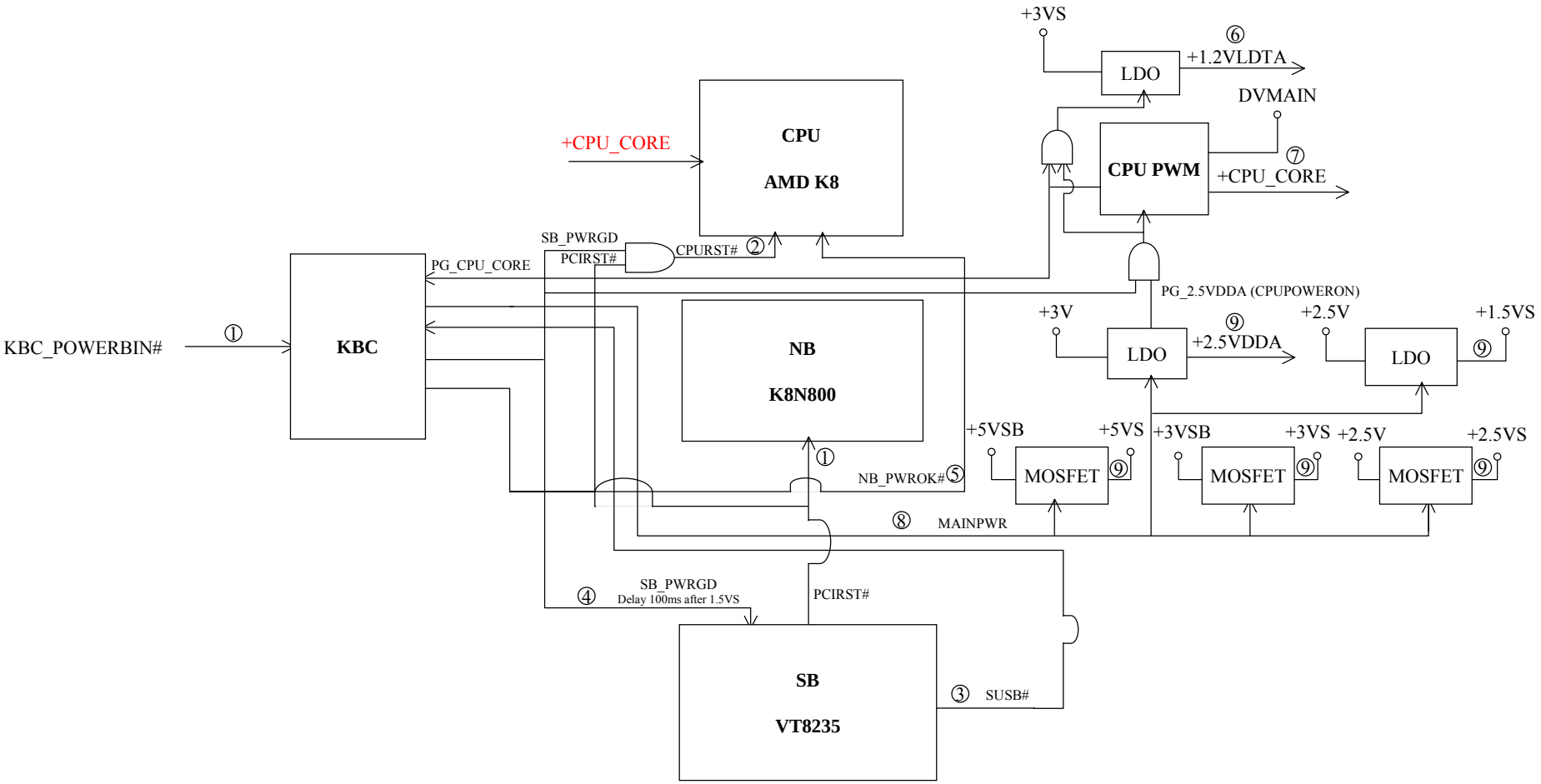
## 1.3.1 Power On Sequence



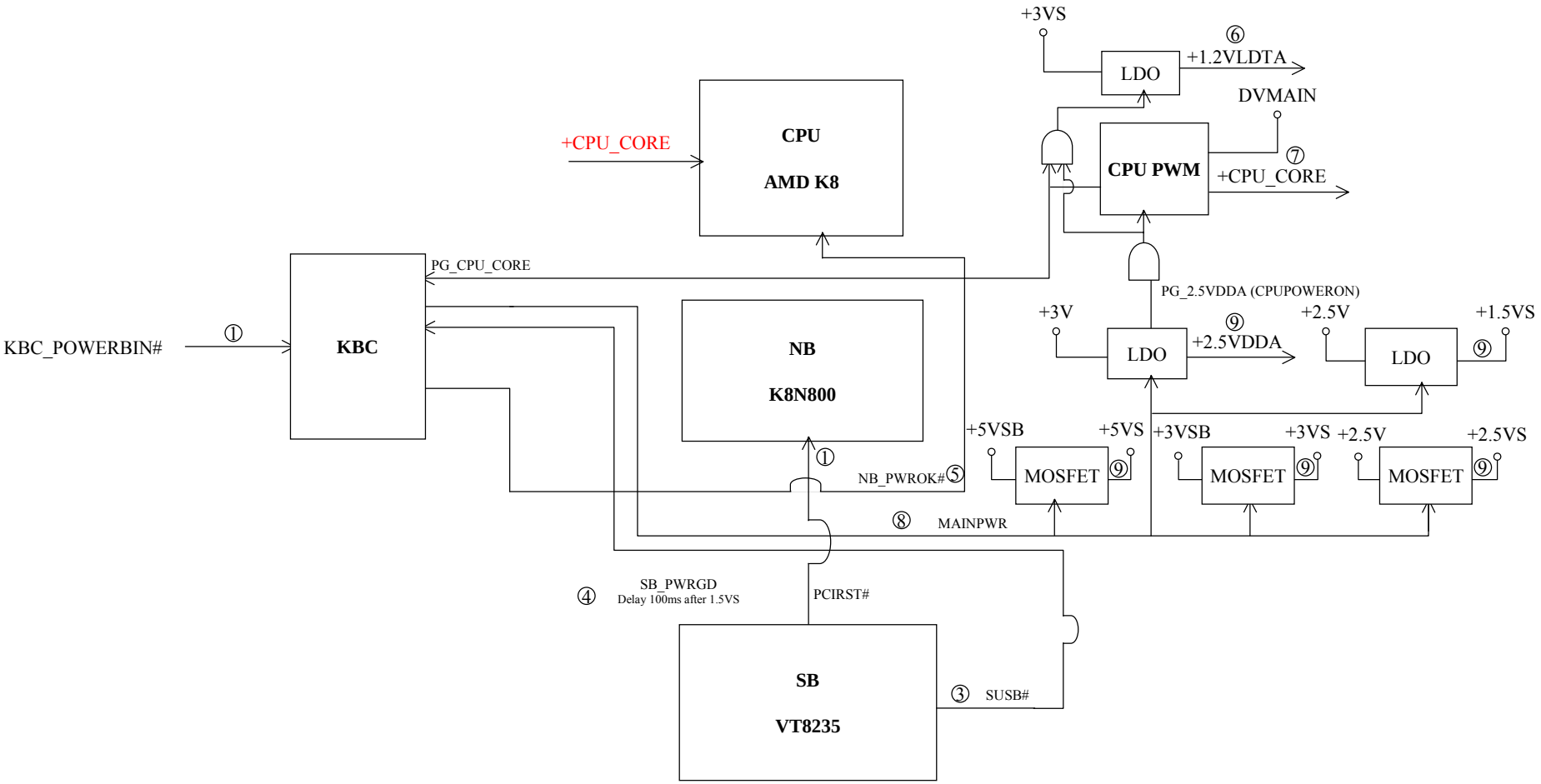
## 1.3.2 Power Off Sequence



## 1.3.3 Suspend To RAM Sequence



## 1.3.4 Resume from Suspend To RAM Sequence



## 1.3.5 Power Consumption Of Suspend Mode

- Suspend to RAM <100mA
- Suspend to Disk / Soft-Off /Mechanical Off < 1mA

## 1.4 Appendix 1: VT8235 GPI/O Pin Define (1)

| Pin Name | Pin# | Mux Function | GPIO Function | Power Plane | Signal Name | Type | Operation |
|---|---|---|---|---|---|---|---|
| GPI0 | AE2 | | GPI | VBAT | GPI0 | | PULL_UP TO VCC_RTC |
| GPO0 | AA3 | | GPO | VSUS33 | GPO0 | | PULL_UP |
| GPI1 | AC2 | | GPI | VSUS33 | SCI# | INPUT | PULL_UP(RESERVE) |
| GPO1 | AA2 | SUSA# | GPO | VSUS33 | SUSA# | MUX FUNC | PULL_UP(RESERVE) |
| GPI2 | AA1 | EXTSMI# | GPI | VSUS33 | EXTSMI# | MUX FUNC | PULL_UP |
| GPO2 | AD3 | SUSB# | GPO | VSUS33 | SUSB# | MUX FUNC | PULL_UP(RESERVE) |
| GPI3 | Y2 | RING# | GPI | VSUS33 | WAKE_UP# | MUX FUNC | PULL_UP |
| GPO3 | Y3 | SUSST1# | GPO | VSUS33 | SB_SUSST# | MUX FUNC | PULL_UP |
| GPI4 | AC1 | LID# | GPI | VSUS33 | LID_SW# | MUX FUNC | |
| GPO4 | AB3 | SUSCLK | GPO | VSUS33 | SPK_OFF | OUTPUT | PULL_UP |
| GPI5 | V4 | BATLOW# | GPI | VSUS33 | CARD_RI# | INPUT | PULL_UP |
| GPO5 | AC7 | CPUSTP# | GPO | MAIN | CPUSTP# | OUTPUT | PULL_UP |
| GPI6 | AD10 | AGPBZ# | GPI | MAIN | AGPBUSY# | MUX FUNC | PULL_UP |
| GPO6 | AD6 | PCISTP# | GPO | MAIN | PCISTP# | MUX FUNC | PULL_UP |
| GPI7 | R3 | REQ5# | GPI | MAIN | PCI_REQ5# | MUX FUNC | PULL_UP |
| GPO7 | R2 | GNT5# | GPO | MAIN | PCI_GNT5# | MUX FUNC | PULL_UP |
| GPIO12 | D4 | INTE# | GPIO | MAIN | PCI_INTE# | MUX FUNC | PULL_UP |
| GPIO13 | B4 | INTF# | GPIO | MAIN | PCI_INTF# | MUX FUNC | PULL_UP |
| GPIO14 | A3 | INTG# | GPIO | MAIN | PCI_INTG# | MUX FUNC | PULL_UP |
| GPIO15 | B3 | INTH# | GPIO | MAIN | PCI_INTH# | MUX FUNC | PULL_UP |
| GPI16 | AE1 | INTRUDER# | GPI | VBAT | GPI16 | | PULL_UP TO VCC_RTC |
| GPI17 | Y1 | CPUMISS | GPI | MAIN | GPI17 | | PULL_UP |
| GPI18 | Y4 | THRM#/AOLGPI | GPI | MAIN | THRM# | MUX FUNC | PULL_DOWN |
| GPIO20 | U1 | ACSDIN2/PCS0# | GPIO | MAIN | SDIN2 | MUX FUNC | PULL_DOWN |
| GPIO21 | V3 | ACSDIN3/PCS1#/SLPBTN# | GPIO | MAIN | SDIN3 | OUTPUT | PULL_UP |
| GPIO22 | R22 | GHI# | GPIO/OD | MAIN | MINIPCI_PD | INPUT | PULL_UP |
| GPIO23 | P21 | DSLP# | GPIO/OD | MAIN | MPCLACT# | MUX FUNC | PULL_UP |

# 1.4 Appendix 1: VT8235 GPI/O Pin Define (2)

Continue to the previous page

| Pin Name | Pin# | Mux Function | GPIO Function | Power Plane | Signal Name | Type | Operation |
|---|---|---|---|---|---|---|---|
| GPIO26 | AD1 | SMBDT2 | GPIO/OD | VSUS33 | SMBDATA | MUX FUNC | PULL_UP |
| GPIO27 | AC3 | SMBCK2 | GPIO/OD | VSUS33 | SMBCLK | | PULL_UP |
| GPIO28 | AC8 | GPIO28 | GPIO/OD | MAIN | VIDSEL | | PULL_POWN |
| GPIO29 | AB9 | VRDSLP | GPIO/OD | MAIN | VRDSLP | | PULL_POWN |

## 1.5 Appendix 2: Keyboard Controller Pin Define (1)

| Pin | Port | Signal Name | Type | Connect To | Description |
|---|---|---|---|---|---|
| 39~54 | GP17~GP0 | KO[0..15] | O | Internal Keyboard | Keyboard Matrix |
| 55~62 | GP37~GP30 | KI[7..0] | O | Internal Keyboard | Keyboard Matrix |
| 65~68 | GP85~GP82 | LAD[0..3] | I/O | VT8235 | LPC BUS |
| 70 | GP80 | PCI_KBCLK | I | CLKGEN | LPC CLK |
| 69 | GP81 | SERIRQ | O | VT8235 | Serial IRQ |
| 64 | GP86 | KBCLRST# | I | VT8235 | LPC Reset |
| 63 | GP87 | LFRAME# | I/O | VT8235 | LPC FRAME |
| 17 | GP50 | MAINPWR | O | W83L950D | We use this signal to control "VS" power on/off. HI:ON,LOW:OFF |
| 15 | GP52 | SUSB# | I | VT8235 | STR Indicator signal |
| 14 | GP53 | ADEN# | I | DC TO DC | ADAPTOR IN |
| 23 | GP42 | NUM_LOCK# | O | LED | Keyboard NUMBERI Lock indicator |
| 22 | GP43 | LID_SW# | I | | panel close |
| 19 | GP46 | SCI | O | VT8235 | Connect to South Bridge (VT8235) to system configuration interrupt (ACPI mode) |
| 3 | GP76 | BAT_DATA | I/O | BAT & LM86 | SMBUS DATA for LM86 themal sensor & BATT THERMAL |
| 2 | GP77 | BAT_CLK | I/O | BAT & LM86 | SMBUS CLK for LM86 themal sensor & BATT THERMAL |
| 27 | GP40 | FAN_ON# | O | CPU FAN | Control CPU FAN ON & Tum ON/OFF Duty |
| 26 | GP41 | | | | |
| 13 | GP54 | FAN0_SPD | I | CPU FAN | Return FAN (CPU FAN) Speed |
| 12 | GP55 | CHG_ON | O | Charge Circuitry | |
| 16 | GP51 | BATT_DEAD | I | Power Circuitry | Indicated the battery capacity is not enough to power on system |
| 18 | GP47 | PWR_ON | O | DC TO DC | Control System Power ON/OFF |
| 21 | GP44 | RCIN# | O | VT8235 | Keyboard Reset for CPURST# gerneration |
| 20 | GP45 | A20GATE | O | VT8235 | GATE A20 OUTPUT |
| 9 | GP70 | T_DATA | I/O | Touch PAD | Conneter to touch Pad DATA |
| 8 | GP71 | LEARNING | O | | |
| 7 | GP72 | SB_PWRBTN# | O | VT8235 | Power Button Signal to VT8235 |
| 6 | GP73 | T_CLK | I/O | Touch PAD | Connect to Touch Pad clock |
| 5 | GP74 | SB_PWRGD | O | VT8235 | System Power Good |

# 1.5 Appendix 2: Keyboard Controller Pin Define (2)

Continue to the previous page

| Pin | Port | Signal Name | Type | Connect To | Description |
|---|---|---|---|---|---|
| 4 | GP75 | SUSB# | I | VT8235 | System inter S4~S5,Positive Logic |
| 38 | GP20 | THRM# | O | VT8235 | TO VT8235,Regustang the sysytem toenter power mangmentmode,Clock Throtting |
| 37 | GP21 | WAKE_UP# | O | VT8235 | Connect to South Bridge (VT8235) to wake up system |
| 36 | GP22 | BATT_G# | O | LED | The indicator when battery in charging |
| 35 | GP23 | BATT_R# | O | LED | The indicator when battery in charging |
| 34 | GP24 | EXTSM# | O | VT8235 | Connect to South Bridge (VT8235) to system management interrupt (Non-ACPI mode) |
| 33 | GP25 | CAP_LOCK# | O | LED | Keyboard CAP lock indicator |
| 32 | GP26 | SCROLL# | O | LED | Keyboard scroll lock indicator |
| 31 | GP27 | AC_BAT_LED# | O | LED | The indicator when power supply from AC-Adapter |
| 11 | GP56 | BLADJ | O | Inverter | Back/Light Adijust Control |
| 10 | GP57 | | | | |
| 1 | GP60 | KBC_PWRBTN# | I | POWER SW | Power Switch Signal to H8 |
| 80 | GP61 | PG_CPU_CORE | I | IMVP IV | indicated the cpu power good |
| 79 | GP62 | | I | 3V | indicated 3V ok |
| 78 | GP63 | BAT_TEMP | I | Battery | Report Battery Thermal |
| 77 | GP64 | BAT_VOLT | I | Battery | Report Battery Voltage |
| 76 | GP65 | I_LIMIT | I | CHARGE | FOR BATTERY CHARGE |
| 75 | GP66 | I_CHG | O | CHARGE | |
| 74 | GP67 | I_DISCHG | I | CHARGE | |
| 25 | RESET# | KBCRST# | | | |
| 28 | XIN | | I | | |
| 29 | XOUT | EXTSMI# | O | VT8235 | Connect to South (VT8235) to system management interruput (Non-ACPI Mode) |
| 72 | VREF | +3VA | | | |
| 71 | VCC | +5VA | | | |

## 1.6 Appendix 3: Audio Performance

8889 meet all the following items

Table 9. Digital Playback (PC-D-A) for Line Output

| Test Items | Mobile System |
|---|---|
| Full Scale Output Voltage | ≧0.7Vrms (3.3V audio) |
| Sample Frequency Accuracy | ≦0.1% |
| Frequency Response (44.1ks/sec) | 20Hz～15kHz |
| Frequency Response (48ks/sec) | 20Hz～15kHz |
| Dynamic Range (SNR) | ≧70dBFSA |
| THD+N | ≦-55dBFS |
| Cross-talk | ≧50dB |

Table 10. Analog Pass-through(A-A) for Microphone Input to Line Output

| Test Items | Mobile System |
|---|---|
| Frequency Response | 100Hz～12kHz |
| Dynamic Range (SNR) | ≧60dBFSA |
| THD+N | ≦-50dBFS |

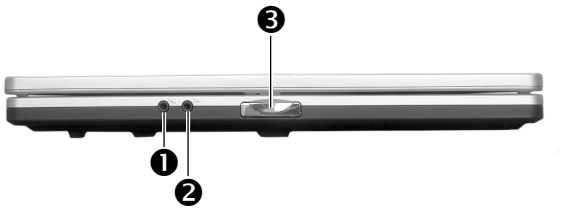
Table 11. Digital Recording(A-D-PC) for Microphone Input

| Test Items | Mobile System |
|---|---|
| Full Scale Input Voltage | ≧100mVrms |
| Sample Frequency Accuracy | ≦0.1% |
| Frequency Response(22.05ks/sec) | 100Hz～8.8kHz |
| Dynamic Range (SNR) | ≧60dBFSA |
| THD+N | ≦-50dBFS |

# 2. System View and Disassembly

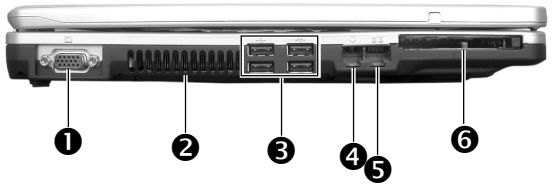
## 2.1 System View

### 2.1.1 Front View




❶ MIC In Connector
❷ Line Out Connector
❸ Top Cover Latch

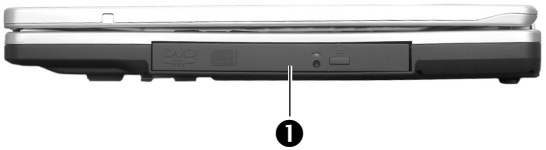
### 2.1.2 Left-side View




❶ VGA Port
❷ Ventilation Openings
❸ USB Ports *4
❹ RJ-11 Connector
❺ RJ-45 Connector
❻ PCMCIA Card Socket

## 2.1.3 Right-side View

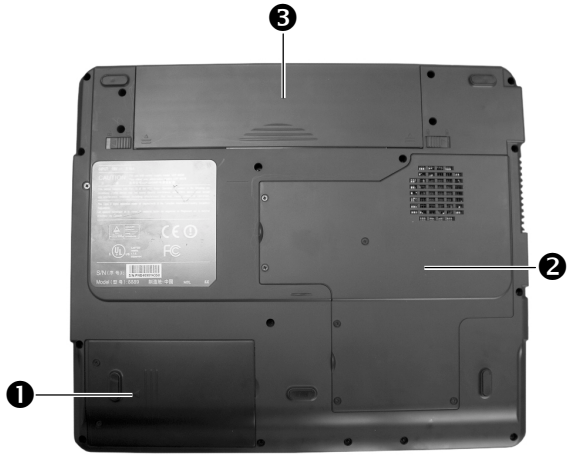
❶ CD-ROM/DVD-ROM Drive




## 2.1.4 Rear View

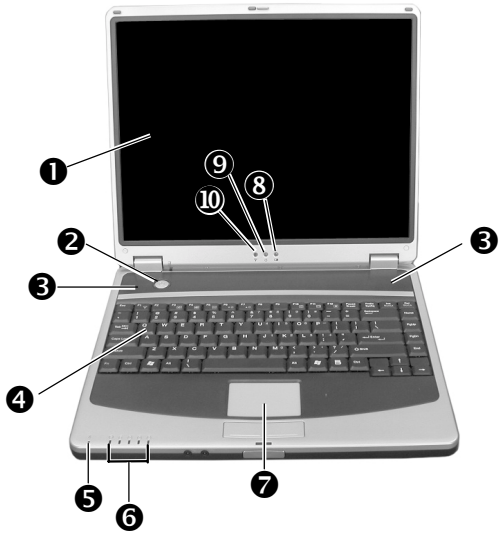
❶ Kensington Lock
❷ Power Connector
❸ S-Video Port

## 2.1.5 Bottom View




❶ Hard Disk Drive
❷ CPU
❸ Battery Park

## 2.1.6 Top-open View

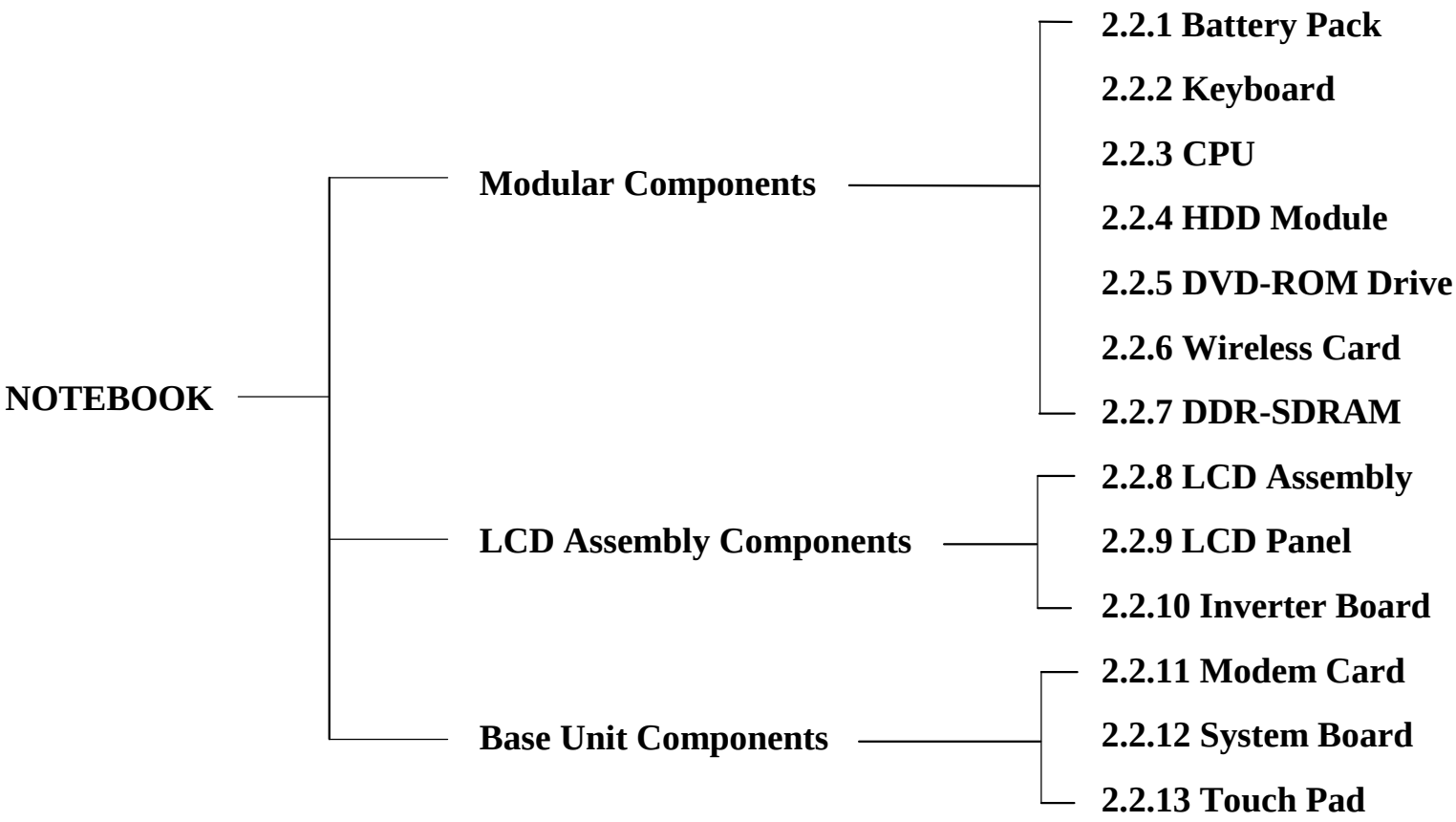



❶ LCD Screen
❷ Power Button
❸ Stereo Speaker Set
❹ Keyboard
❺ Internal MIC In
❻ Device LED Indicators
❼ Touch Pad
❽ Battery Charge Indicator
❾ Power Indicator
❿ Wireless Card Indicator

## 2.2 System Disassembly

The section discusses at length each major component for disassembly/reassembly and show corresponding illustrations.Use the chart below to determine the disassembly sequence for removing components from the notebook.

***NOTE:*** *Before you start to install/replace these modules, disconnect all peripheral devices and make sure the notebook is not turned on or connected to AC power.*



## 2.2.1 Battery Pack

### Disassembly

1. Carefully put the notebook upside down.
2. Slide the two release lever outwards to the "unlock" ( ) position (❶), while take the battery pack out of the compartment (❷). (Figure 2-1)

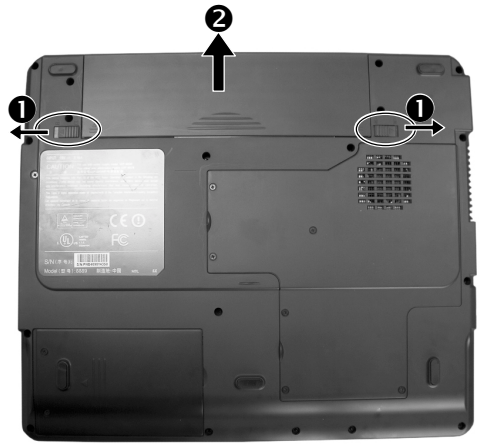



Figure 2-1 Remove the battery pack

### Reassembly

1. Replace the battery pack into the compartment. The battery pack should be correctly connected when you hear a clicking sound.
2. Slide the release lever to the "lock" ( ) position.

## 2.2.2 Keyboard

### Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Push the keyboard cover to loose the locks from the battery compartment. (Figure 2-2)
3. Lift the keyboard cover up. (Figure 2-3)

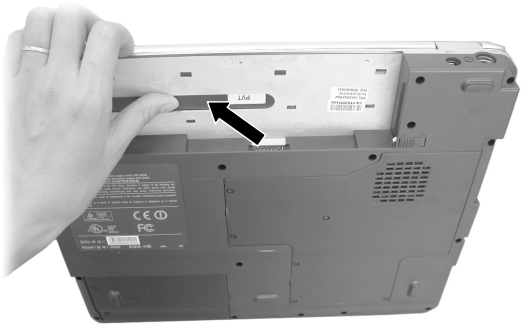


Figure 2-2 Push the keyboard cover

Figure 2-3 Lift the keyboard cover

4. Slightly lift up the keyboard. (Figure 2-4)
5. Disconnect the cable from the system board, then separate the keyboard. (Figure 2-5)

Figure 2-4 Lift the keyboard

Figure 2-5 Disconnect the cable

**Reassembly**

1. Reconnect the keyboard cable and fit the keyboard back into place.
2. Replace the keyboard cover.
3. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

## 2.2.3 CPU

### Disassembly

1. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove the six screws fastening the CPU cover. (Figure 2-6)
3. Remove the four spring screws that secure the heatsink upon the CPU and disconnect the fan's power cord from system board. (Figure 2-7)

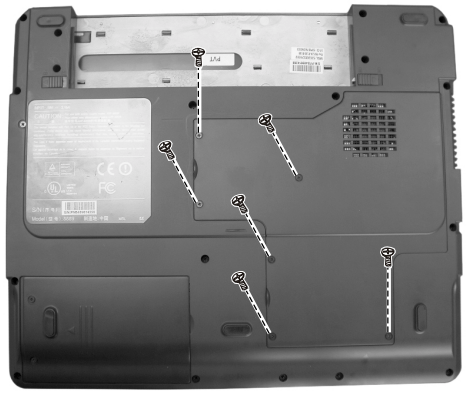


Figure 2-6 Remove the six screws

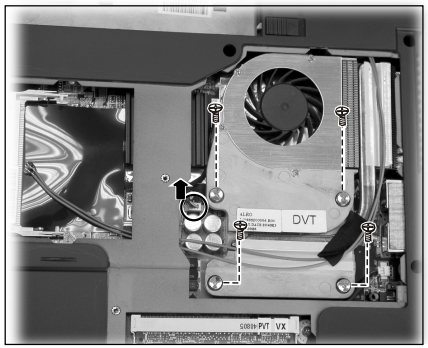



Figure 2-7 Free the heatsink

4. To remove the existing CPU, loosen the screw by a flat screwdriver, upraise the CPU socket to unlock the CPU. (Figure 2-8)

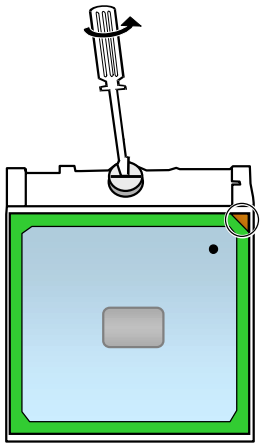


Figure 2-8 Remove the CPU

**Reassembly**

1. Carefully, align the arrowhead corner of the CPU with the beveled corner of the socket, then insert CPU pins into the holes. Tighten the screw by a flat screwdriver to locking the CPU.
2. Connect the fan's power cord to the system board, fit the heatsink upon the CPU and secure with four spring screws.
3. Replace the CPU cover and secure with six screws.
4. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

## 2.2.4 HDD Module

### Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove the two screws fastening the HDD compartment cover. (Figure 2-9)
3. Remove the one screw and slide the HDD module out of the compartment. (Figure 2-10)

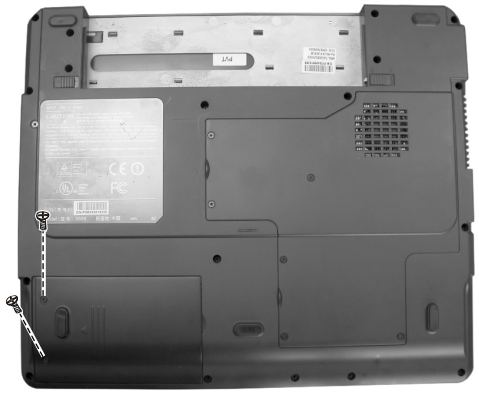


Figure 2-9 Remove the HDD compartment cover

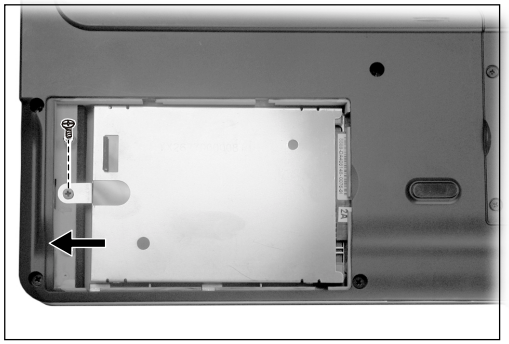


Figure 2-10 Remove HDD module

4. Remove the four screws to separate the hard disk drive from the bracket, remove the hard disk drive. (Figure 2-11)

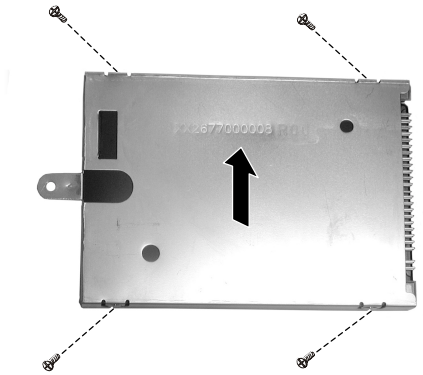


Figure 2-11 Remove hard disk drive

**Reassembly**

1. Attach the bracket to hard disk drive and secure with four screws.
2. Slide the HDD module into the compartment and secure with one screw.
3. Place the HDD compartment cover and secure with two screws.
4. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

## 2.2.5 CD/DVD-ROM Drive

### Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to section 2.2.1 Disassembly)
2. Remove the one screw fastening the CD/DVD-ROM drive. (Figure 2-12)
3. Insert a small rod, such as a straightened paper clip, into CD/DVD-ROM drive's manual eject hole (❶) and push firmly to release the tray. Then gently pull out the CD/DVD-ROM drive by holding the tray that pops out (❷). (Figure 2-12)

Figure 2-12 Remove the CD/DVD-ROM drive

### Reassembly

1. Push the CD/DVD-ROM drive into the compartment and secure with one screw.
2. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

## 2.2.6 Wireless Card

### Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (Refer to sections 2.2.1 Disassembly)
2. Remove the six screws fastening the CPU cover. (Refer to step 2 of section 2.2.3 Disassembly)
3. Disconnect the wireless card's antennae first (❶). Then pull the retaining clips outwards (❷) and remove the wireless card (❸). (Figure 2-13)

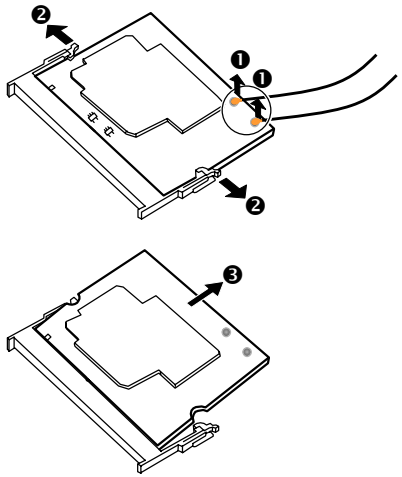



Figure 2-13 Remove the Wireless card

### Reassembly

1. To install the wireless card, match the wireless card 's notched part with the socket's projected part and firmly insert it into the socket. Then push down until the retaining clips lock the wireless card into position. Then sure that the antennae fully populated.
2. Replace the CPU cover and secure with six screws. (Refer to step 3 of section 2.2.3 Reassembly)
3. Replace the battery pack. (Refer to section 2.2.1 Reassembly)

## 2.2.7 DDR-SDRAM

### Disassembly

1. Carefully put the notebook upside down. Remove the battery pack. (See section 2.2.1 Disassembly)
2. Remove the six screws fastening the CPU cover. (Refer to step 2 of section 2.2.3 Disassembly)

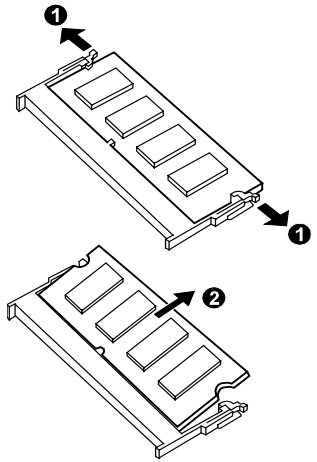



Figure 2-14 Remove the SO-DIMM

3. Pull the retaining clips outwards (❶) and remove the SO-DIMM (❷). (Figure 2-14)

### Reassembly

1. To install the DDR, match the DDR's notched part with the socket's projected part and firmly insert the SO-DIMM into the socket at 20-degree angle. Then push down until the retaining clips lock the DDR into position.
2. Replace the CPU cover and secure with six screws. (Refer to step 3 of section 2.2.3 Reassembly)
3. Replace the battery pack. (See section 2.2.1 Reassembly)

## 2.2.8 LCD ASSY

### Disassembly

1. Remove the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, wireless card and DDR. (See sections 2.2.1,2.2.2, 2.2.3, 2.2.4, 2.2.5, 2.2.6 and 2.2.7 Disassembly)
2. Remove the two screws fastening the housing. (Figure 2-15)
3. Remove the twenty-two screws, then free the housing. (Figure 2-16)

Figure 2-15 Remove the two screws

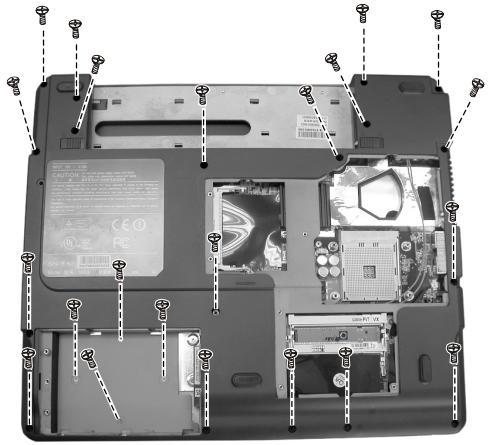


Figure 2-16 Free the housing

4. Remove the two hinge covers. (Figure 2-17)
5. Disconnect the four cables from the system board. (Figure 2-18)

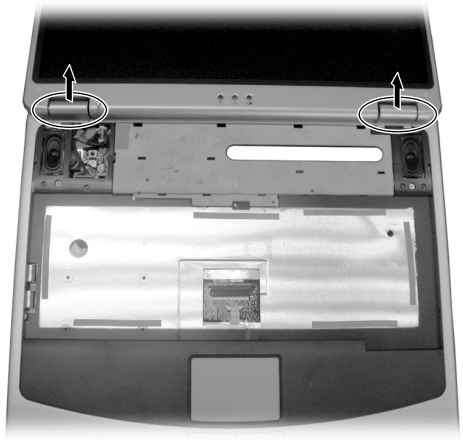


Figure 2-17 Remove the hinge covers

Figure 2-18 Disconnect the four cables

6. Disconnect the one cable from the system board, then remove the two screws and two hex nuts. And free the system board. (Figure 2-19)
7. Remove the four screws, then free the LCD assembly. (Figure 2-20)

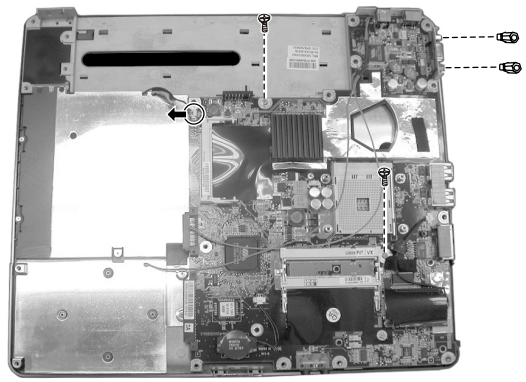


Figure 2-19 Free the system board

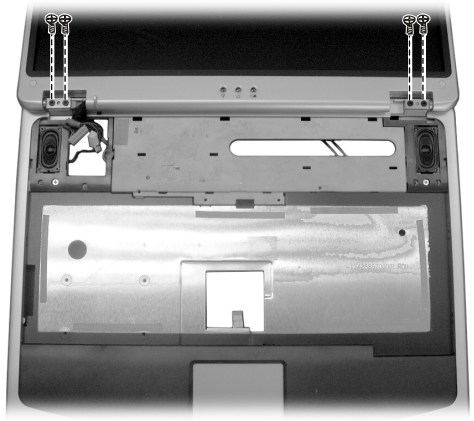


Figure 2-20 Free the LCD assembly

**Reassembly**

1. Attach the LCD assembly to the base unit and secure with four screws.
2. Replace the antenna wires.
3. Replace the system board back into the top cover, then secure with two screws and two hex nuts.
4. Reconnect the five cables to the system board.
5. Replace the housing and secure with twenty-four screws.
6. Replace the two hinge covers.
7. Replace the DDR, wireless card, CD/DVD-ROM drive, hard disk drive, CPU, keyboard and battery pack. (Refer to sections 2.2.7, 2.2.6, 2.2.5, 2.2.4, 2.2.3, 2.2.2 and 2.2.1 Reassembly)

## 2.2.9 LCD Panel

**Disassembly**

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, wireless card, DDR and LCD assembly. (Refer to section 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5, 2.2.6, 2.2.7 and 2.2.8 Disassembly)
2. Remove the two rubber pads and two screws on the corners of the panel. (Figure 2-21)
3. Insert a flat screwdriver to the lower part of the LCD cover and gently pry the frame out. Repeat the process until the cover is completely separated from the housing.
4. Remove the six screws and disconnect the cable. (Figure 2-22)

Figure 2-21 Remove LCD cover

Figure 2-22 Remove the six screws and disconnect the cable

5. Remove the four screws that secure the LCD brackets. (Figure 2-23)
6. Disconnect the cable to free the LCD panel. (Figure 2-24)

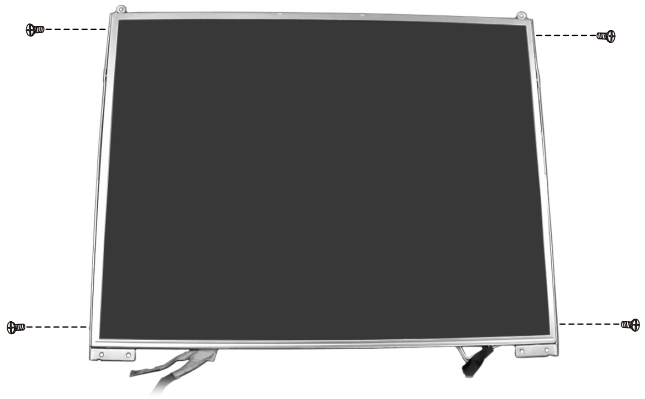


Figure 2-23 Remove the four screws

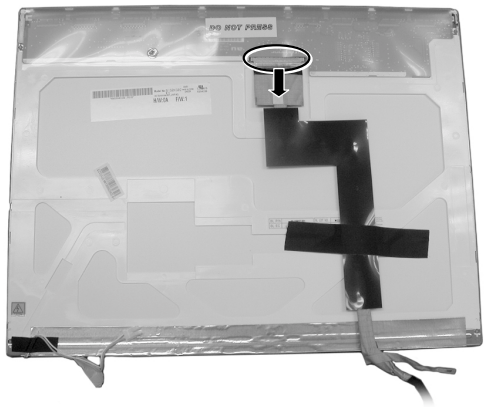


Figure 2-24 Free the LCD panel

**Reassembly**

1. Replace the cable to the LCD panel.
2. Attach the LCD panel's brackets back to LCD panel and secure with four screws.
3. Replace the LCD panel into LCD housing. And reconnect one cable to inverter board.
4. Fasten the LCD panel by six screws.
5. Fit the LCD cover and secure with two screws and rubber pads.
6. Replace the LCD assembly, DDR, wireless card, CD/DVD-ROM drive, hard disk drive, CPU, keyboard and battery pack. (See sections 2.2.8, 2.2.7, 2.2.6, 2.2.5, 2.2.4, 2.2.3, 2.2.2 and 2.2.1 Reassembly)

## 2.2.10 Inverter Board

### Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, wireless card, DDR and LCD assembly. (Refer to section 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5, 2.2.6, 2.2.7 and 2.2.8 Disassembly)
2. Remove the LCD cover. (Refer to the steps 1-3 of section 2.2.10 Disassembly )
3. Remove the two screws fastening the inverter board and disconnect the cable, then free the inverter board. (Figure 2-25)

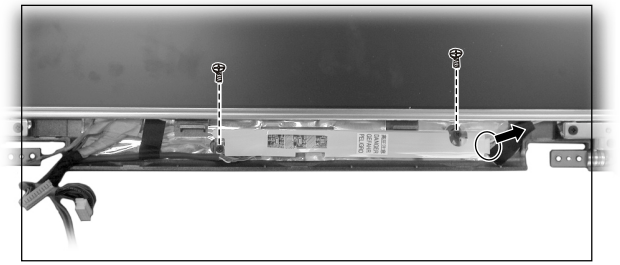


Figure 2-25 Free the inverter board

### Reassembly

1. Reconnect the cable. Fit the inverter board back into place and secure with two screws.
2. Replace the LCD cover. (Refer to section 2.2.9 Reassembly)
3. Replace the LCD assembly. (Refer to section 2.2.8 Reassembly)
4. Replace the DDR, wireless card, CD/DVD-ROM drive, hard disk drive, CPU, keyboard and battery pack. (Refer to sections 2.2.7, 2.2.6, 2.2.5, 2.2.4, 2.2.3, 2.2.2 and 2.2.1 Reassembly)

## 2.2.11 Modem Card

### Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, wireless card and DDR-SDRAM. (Refer to sections 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5, 2.2.6 and 2.2.7 Disassembly)
2. Remove the housing. (Refer to the steps 2-3 of section 2.2.8 Disassembly)
3. Disconnect the cable from the system board, then remove the two screws fastening the modem card. (Figure 2-26)

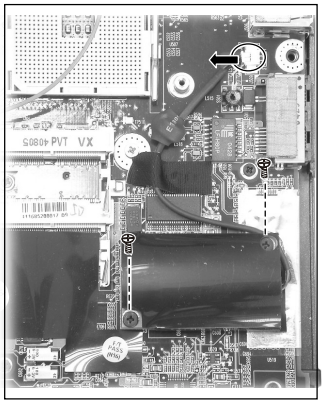


Figure 2-26 Free the modem card

### Reassembly

1. Replace the modem card and secure with two screws.
2. Reconnect the cable.
3. Replace the housing. (Refer to the step 5 of section 2.2.8 Reassembly)
4. Replace the DDR-SDRAM, wireless card, CD/DVD-ROM, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

## 2.2.12 System Board

### Disassembly

1. Remove the battery, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, wireless card, DDR-SDRAM and modem card. (Refer to sections 2.2.1, 2.2.2, 2 .2.3, 2.2.4, 2.2.5, 2.2.6, 2.2.7 and 2.2.11 Disassembly)
2. Disconnect the four cables from the system board. (Figure 2-27)
3. Disconnect the one cable from the system board, then remove the two screws and two hex nuts. And lift the system board from the top cover, free the system board. (Figure 2-28)

Figure 2-27 Disconnect the four cables

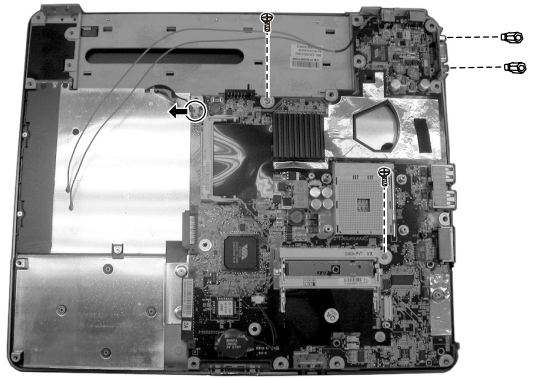


Figure 2-28 Free the system board

### Reassembly

1. Replace the system board back into the top cover. Secure with two screws and two hex nuts.
2. Reconnect the L/R speakers' cables, touch pad's cable, LCD panel's cable and inverter board's cable.
3. Replace the modem card, DDR-SDRAM, wireless card, CD/DVD-ROM, hard disk drive, CPU, keyboard and battery pack. (Refer to previous section reassembly)

## 2.2.13 Touch Pad

### Disassembly

1. Remove the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, wireless card, DDR-SDRAM and LCD assembly. (See sections 2.2.1, 2.2.2, 2.2.3, 2.2.4, 2.2.5, 2.2.6, 2.2.7 and 2.2.8 Disassembly)
2. Remove the two screws fastening the touch pad button. (Figure 2-29)
3. Remove the thirteen screws and lift the shielding, then free the touch pad. (Figure 2-30)

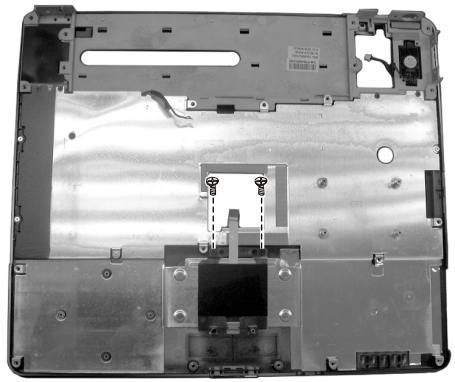


Figure 2-29 Remove the two screws

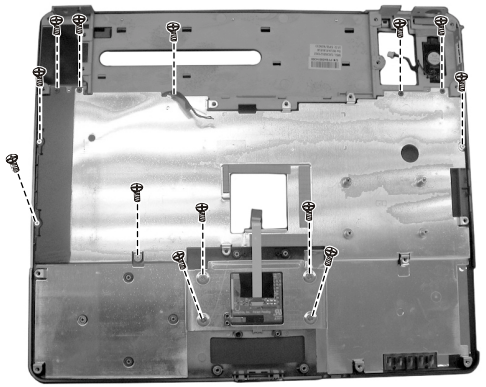


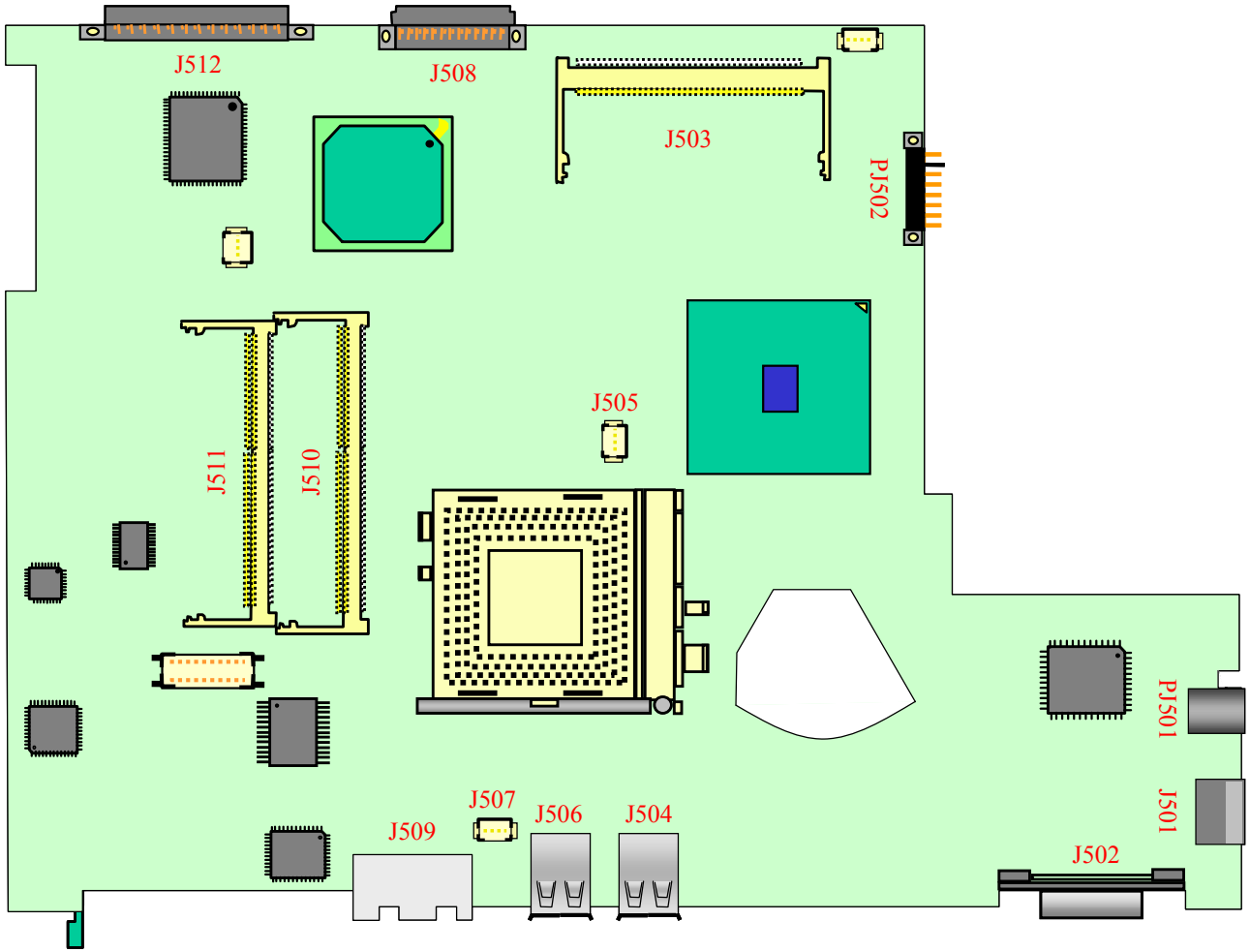
Figure 2-30 Free the touch pad

### Reassembly

1. Replace the touch pad, then fit the shielding and secure with thirteen screws.
2. Replace the touch pad button back into the top cover and secure with two screws.
3. Replace the battery pack, keyboard, CPU, hard disk drive, CD/DVD-ROM drive, wireless card, LCD assembly, the modem card and the system board. (See sections previous section reassembly)

# 3. Definition & Location of Connectors / Switches

## 3.1 Mother Board (Side A) - 1

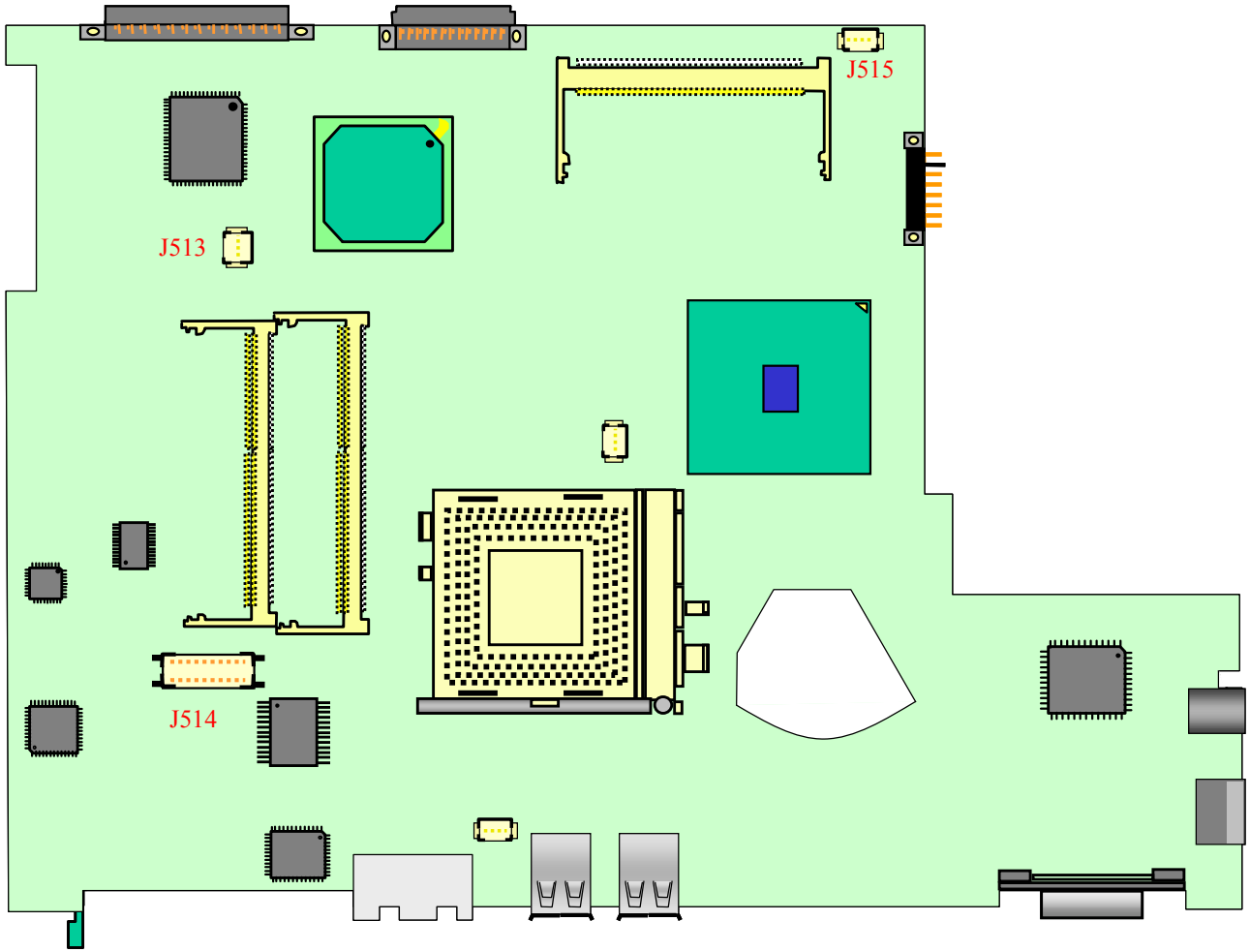



- PJ501 : AC Power Jack
- PJ502 : Battery Connector
- J501 : S-Video Port
- J502 : External VGA Connector
- J503 : Mini-PCI Socket
- J504,J506 : USB Port
- J505 : CPU Fan Connector
- J507 : MDC Jump Wire Connector
- J508 : Secondary IDE Connector
- J509 : RJ11 & RJ45 Connector
- J510,J511 : Extend DDR SDRAM Socket
- J512 : Primary EIDE Connector

------ To next page ------

# 3. Definition & Location of Connectors / Switches

## 3.1 Mother Board (Side A) - 2

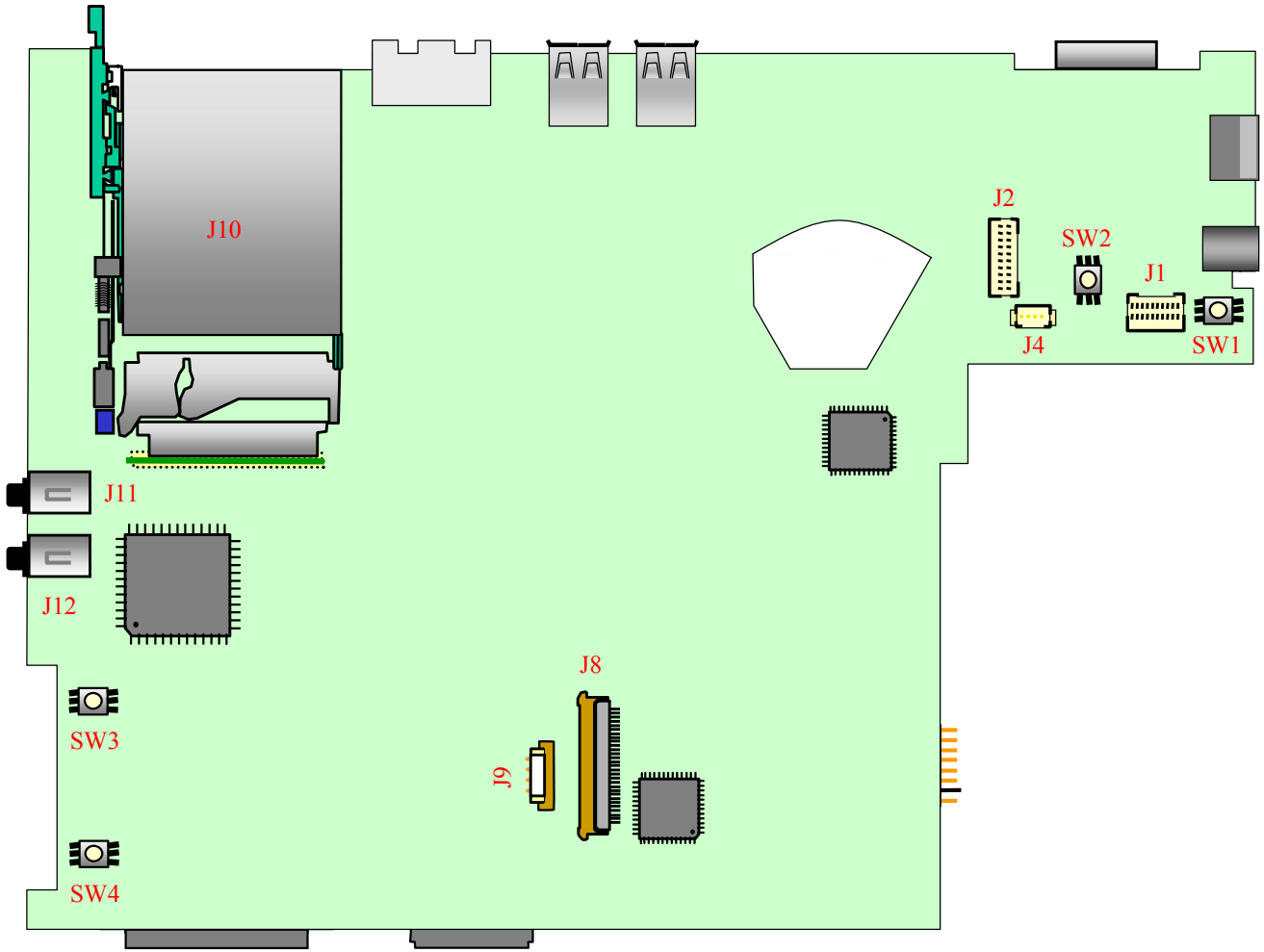



------ Continued to previous page ------

- J513 : RTC Battery Connector
- J514 : MDC Board Connector
- J515 : Internal Right Speak Connector

# 3. Definition & Location of Connectors / Switches

## 3.1 Mother Board (Side B)

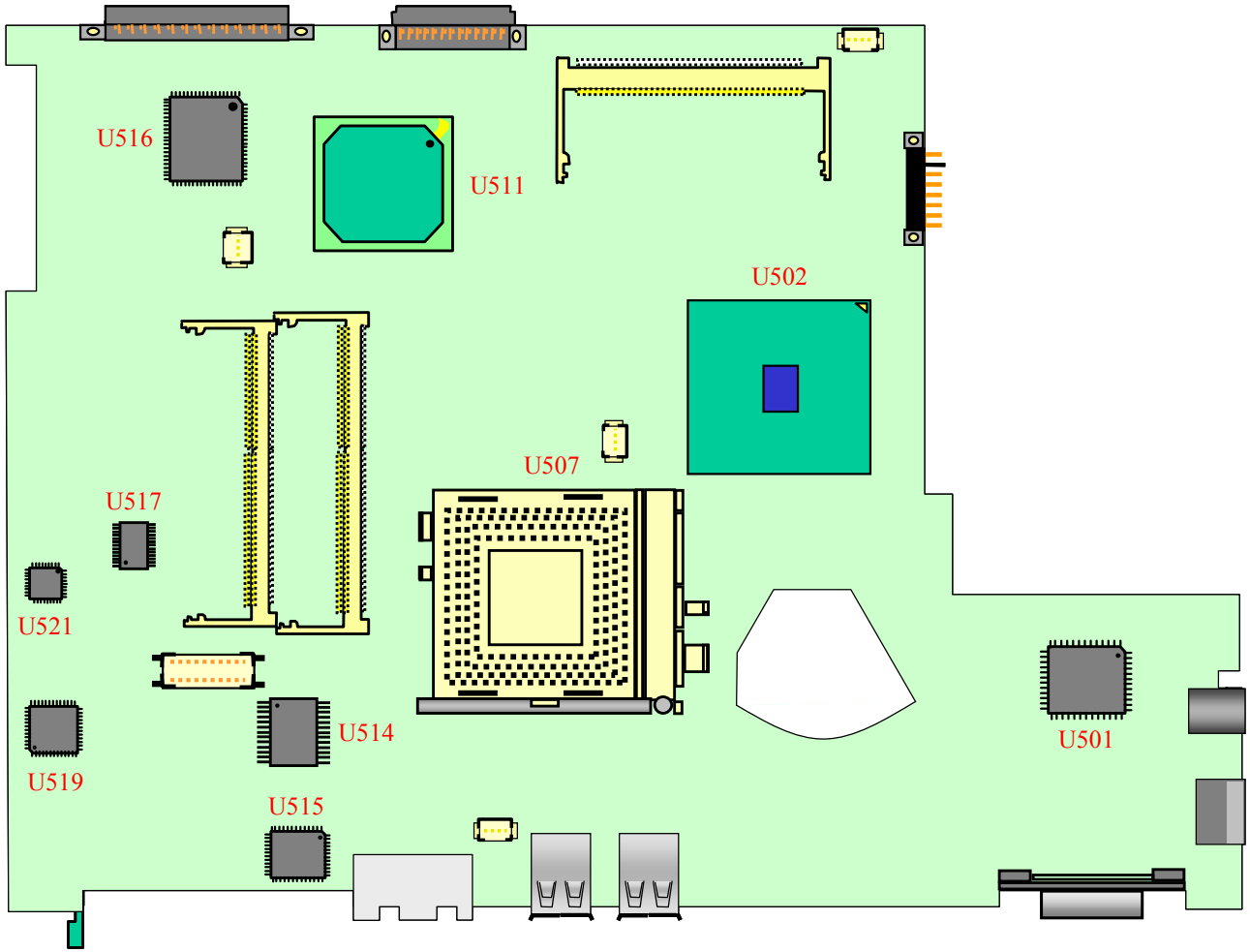



- J1 : LCD Connector
- J2 : LCD Inverter Connector
- J4 : Internal Left Speak Connector
- J8 : Internal Keyboard Connector
- J9 : Touch-Pad Connector
- J10 : PCMCIA Card Socket
- J11 : MIC In Jack
- J12 : Line Out Jack

- SW1 : Dormancy Button
- SW2 : Power Button
- SW3 : Touch-Pad Left Button
- SW4 : Touch-Pad Right Button

# 4. Definition & Location of Major Components

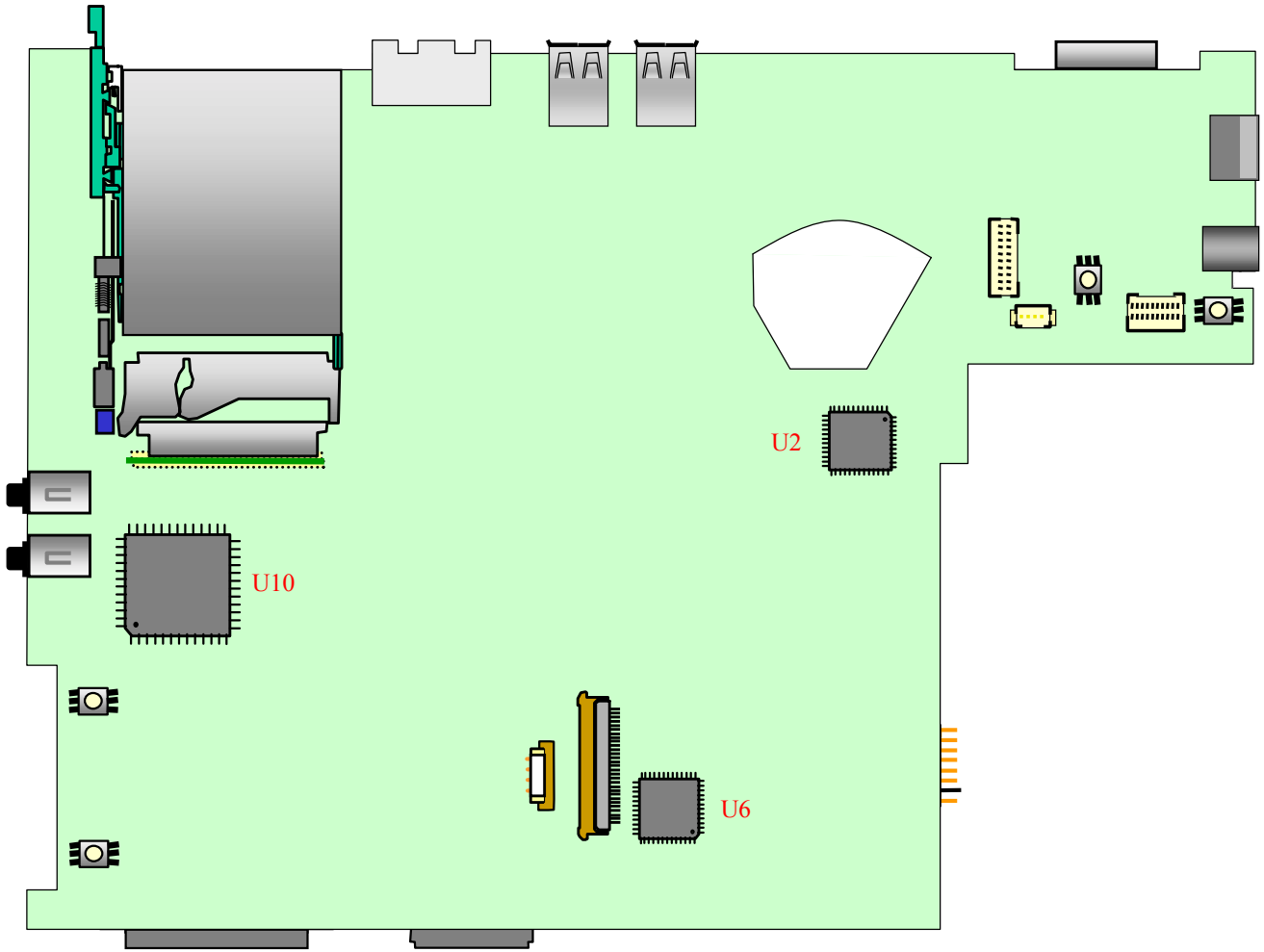
## 4.1 Mother Board (Side A)




- U501 : VT1634 LVDS Transmitter
- U502 : NB VIA_K8N800
- U507 : CPU (AMD Mobile K8) Socket
- U511 : SB VT8235CE
- U514 : ICS952007 Clock Generator
- U515 : VT6103L LAN Controller
- U516 : System BIOS
- U517 : CP2211 Power Switch
- U519 : ALC655 Audio Codec
- U521 : TPA0212_GND Amplifier

# 4. Definition & Location of Major Components

## 4.1 Mother Board (Side B)




- U2 : TV Encoder (VT1623)
- U6 : KBC (W83L950D)
- U10 : ENE CB1410 CardBus

# 5. Pin Descriptions of Major Components

## 5.1 AMD Mobile K8 CPU - 1

### DDR SDRAM Memory Interface Pins

| Signal Name | Type | Description |
|---|---|---|
| MEMCLK_H/L[7] | O-IOD | Differential DDR SDRAM clock to the top of DIMM 0 for unbuffered DIMMs.1 |
| MEMCLK_H/L[6] | O-IOD | Differential DDR SDRAM clock to the top of DIMM 1 for unbuffered DIMMs.1 |
| MEMCLK_H/L[5] | O-IOD | Differential DDR SDRAM clock to the bottom of DIMM 0 for unbuffered DIMMs.1 |
| MEMCLK_H/L[4] | O-IOD | Differential DDR SDRAM clock to the bottom of DIMM 1 for unbuffered DIMMs.1 |
| MEMCLK_H/L[3] | O-IOD | Differential DDR SDRAM clock to DIMM 3 for registered DIMMs.1 |
| MEMCLK_H/L[2] | O-IOD | Differential DDRS DRAM clock to DIMM 2 for registered DIMMs.1 |
| MEMCLK_H/L[1] | O-IOD | Differential DDR SDRAM clock to the middle of DIMM 1 for unbuffered DIMMs, or DIMM 1 for registered DIMMs.1 |
| MEMCLK_H/L[0] | O-IOD | Differential DDR SDRAM clock to the middle of DIMM 0 for unbuffered DIMMs, or DIMM 0 for registered DIMMs.1 |
| MEMCKEA<br>MEMCKEB | O-IOS | Clock Enables to DIMMs. Used to gate clocks for power management functionality.1 |
| MEMDQS[17:0] | B-IOS | DRAM Data Strobes synchronous with MEMDATA and MEMCHECK during DRAM read and writes.1 |
| MEMDATA[63:0] | B-IOS | DRAM Interface Data Bus |
| MEMCHECK[7:0] | B-IOS | DRAM Interface ECC Check Bits |
| MEMCS_L[7:0] | O-IOS | DRAM Chip Selects 1 |
| MEMRASA_L<br>MEMRASB_L | O-IOS | DRAM Row Address Select. MEMRASA_L and MEMRASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1 |
| MEMCASA_L<br>MEMCASB_L | O-IOS | DRAM Column Address Select. MEMCASA_L and MEMCASB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1 |
| MEMWEA_L<br>MEMWEB_L | O-IOS | DRAM Write Enable. MEMWEA_L and MEMWEB_L are functionally identical. Two copies are provided to accommodate the loading of unbuffered DIMMs.1 |

### DDR SDRAM Memory Interface Pins (Continued)

| Signal Name | Type | Description |
|---|---|---|
| MEMADDA[13:0]<br>MEMADDB[13:0] | O-IOS | DRAM Column/Row Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes, the two copies are inverted from each other (except A[10] which is used for auto-precharge) to minimize switching noise. The signals are inverted only when the bus is used to carry address information.1 |
| MEMBANKA[1:0]<br>MEMBANKB[1:0] | O-IOS | DRAM Bank Address. Two copies are provided to accommodate the loading of unbuffered DIMMs. During precharges, activates, reads, and writes the two copies are inverted from each other to minimize switching noise. The signals are inverted only when the bus is used to carry address information.1 |
| MEMRESET_L | O-IOS | DRAM Reset pin for Suspend-to-RAM power management mode. This pin is required for registered DIMMs only. |
| MEMVREF | VREF | DRAM Interface Voltage Reference 1 |
| MEMZP | A | Compensation Resistor tied to VSS 1 |
| MEMZN | A | Compensation Resistor tied to 2.5 V 1 |

***Notes:***

*1. For connection details and proper resistor values, see the* AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665*

### Clock Pin Descriptions

| Signal Name | Type | Description |
|---|---|---|
| CLKIN_H/L | I-IOD | 200-MHz PLL Reference Clock |
| FBCLKOUT_H/L | O-IOD | Core Clock PLL 200-MHz Feedback Clock |

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## Miscellaneous Pin Descriptions

| Signal Name | Type | Description |
|---|---|---|
| RESET_L | I-IOS | System Reset |
| PWROK | I-IOS | Indicates that voltages and clocks have reached specified operation |
| LDTSTOP_L | I-IOS | HyperTransport™ Technology Stop Control Input. Used for power management and for changing HyperTransport link width and frequency. |
| VID[4:0] | O-IOS | Voltage ID to the regulator |
| THERMDA | A | Anode (+) of the thermal diode |
| THERMDC | A | Cathode (–) of the thermal diode |
| THERMTRIP_L | O-IO-OD | Thermal Sensor Trip output, asserted at nominal temperature of 125 ℃. |
| COREFB_H/L | A | Differential feedback for VDD Power Supply |
| VDDIOFB_H/L | A | Differential feedback for VDDIO Power Supply |
| CORE_SENSE | A | VDD voltage monitor pin |
| VDDA | S | Filtered PLL Supply Voltage |
| VTT_SENSE | A | VTT voltage monitor pin |
| VDDIO_SENSE | A | VDDIO voltage monitor pin |
| VDD | S | Core power supply |
| VDDIO | S | DDR SDRAM I/O ring power supply |
| VLDT_A<br>VLDT_B | S | HyperTransport™ I/O ring power supply for side A and side B of the package |
| VTT_A<br>VTT_B | S | VTT regulator voltage for side A and side B of the die |
| VSS | S | Ground |

## Debug Pin Descriptions

| Signal Name | Type | Description |
|---|---|---|
| DBREQ_L | I-IOS | Debug Request |
| DBRDY | O-IOS | Debug Ready |

## HyperTransport™ Technology Pin Descriptions

| Signal Name | Type | Description |
|---|---|---|
| L0_CLKIN_H/L[1:0] | I-HT | Link 0 Clock Input |
| L0_CTLIN_H/L[1:0] | I-HT | Link 0 Control Input 2 |
| L0_CADIN_H/L[15:0] | I-HT | Link 0 Command/Address/Data Input |
| L0_CLKOUT_H/L[1:0] | O-HT | Link 0 Clock Outputs |
| L0_CTLOUT_H/L[1:0] | O-HT | Link 0 Control Output |
| L0_CADOUT_H/L[15:0] | O-HT | Link 0 Command/Address/Data Outputs |
| L0_REF1 | A | Compensation Resistor to VLDT 1 |
| L0_REF0 | A | Compensation Resistor to VSS 1 |

***Notes:***

*1. These pins are used in an alternating fashion to compensate R TT by internal comparison to 3/4 VLDT and 1/4 VLDTand compensate R ON by comparison to each other around 1/2 VLDT. For proper resistor value, see the*AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665.*

*2. The unused L0_CTLIN_H/L[1] pins must be properly terminated such that the true pin is pulled High and thecomplement is pulled Low. Refer to the* AMD Athlon™ 64 Processor Motherboard Design Guide*, order# 24665, for details.*

## JTAG Pin Descriptions

| Signal Name | Type | Description |
|---|---|---|
| TCK | I-IOS | JTAG Clock |
| TMS | I-IOS | JTAG Mode Select |
| TRST_L | I-IOS | JTAG Reset |
| TDI | I-IOS | JTAG Data Input |
| TDO | O-IOS | JTAG Data Output |

# 5.2 K8N800 North Bridge - 1

## AGP Bus Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **GD[31:0]** | (see pin list) | IO | **Address / Data Bus.** Address is driven with GDS assertion for AGP-style transfers and with GFARME# assertion for PCI-style transfers. |
| **GC#BE[3:0]** (GCBE[3:0]# for 4x mode) | AC7<br>AD11<br>AF11<br>AD15 | IO | **Command / Byte Enable.** (Interpreted as GC/BE# for AGP 2x/4x and GC#/BE for 8x). For AGP cycles these pins provide command information (different commands than for PCI) driven by the master (graphics controller) when requests are being enqueued using GPIPE# (2x/4x only as GPIPE# isn™t used in 8x mode). These pins provide valid byte information during AGP write transactions and are driven by the master. The target (this chip) drives these lines to io0000lt during the return of AGP read data. For PCI cycles, commands are driven with GFARME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks. |
| **GPAR** | AC16 | IO | **AGP Parity.** A single parity bit is provided over GD[31:0] and GC#BE[3:0]. |
| **GDBIH** / GPIPE#**GDBIL** | AC5<br><br>AC4 | IO | **Dynamic Bus Inversion High / Low.** AGP 8x transfer mode only. Driven by the source to indicate whether the corresponding data bit group (GDBIH for GD[31:16] and GDBIL for GD[15:0]) needs to be inverted on the receiving end (1 on GDBIx indicates that the corresponding data bit group should be inverted). Used to limit the number of simultaneously switching outputs to 8 for each 16-pin group.<br>**Pipelined Request.** Not used by AGP 8x. Asserted by the master (external graphics controller) to indicate that a full-width request is to be enqueued by the target (North Bridge). The master enqueues one request each rising edge of GCLK while GPIPE# is asserted. When GPIPE# is deasserted no new requests are enqueued across the AD bus.<br>**Note**: See RxAE[1] for GPIPE# / GDBIH pin function selection. |
| **GADSTB0F**(GADSTB0 for 4x), **GADSTB0S**(GADSTB0# for 4x) | AE15<br><br>AF15 | IO | **Bus Strobe 0.** Source synchronous strobes for GD[15:0] (the agent that is providing the data drives these signals). GDS0 provides timing for 2x data transfer mode; GDS0 and GDS0# provide timing for 4x mode. For 8x transfer mode, GDS0 is interpreted as GDS0F (i1Firstl. strobe) and GDS0# as GDS0S (iSSecondl. strobe). |

## AGP Bus Interface (Continued)

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **GADSTB1F**(GADSTB1 for 4x), **GADSTB1S**(GADSTB1# for 4x) | AE7<br><br>AF7 | IO | **Bus Strobe 1.** Source synchronous strobes for GD[31:16] (i.e., the agent that is providing the data drives these signals). GDS1 provides timing for 2x data transfer mode; GDS1 and GDS1# provide timing for 4x transfer mode. For 8x transfer mode, GDS1 is interpreted as GDS1F (iSFirstle strobe) and GDS1# as GDS1S (iSSecondld strobe). |
| **GFRAME**(GFRAME# for 4x) | AC9 | IO | **Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. Interpreted as active high for 8x. |
| **GIRDY**(GIRDY# for 4x) | AC10 | IO | **Initiator Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP write cycles, the assertion of this pin indicates that the master is ready to provide *all* write data for the current transaction. Once this pin is asserted, the master is not allowed to insert wait states. For AGP read cycles, the assertion of this pin indicates that the master is ready to transfer a subsequent block of read data. The master is *never* allowed to insert a wait state during the initial block of a read transaction. However, it may insert wait states after each block transfers. For PCI cycles, asserted when the initiator is ready for data transfer. |
| **GTRDY**(GTRDY# for 4x) | AC14 | IO | **Target Ready.** (Interpreted as active low for PCI/AGP2x/4x and high for AGP 8x). For AGP cycles, indicates that the target is ready to provide read data for the entire transaction (when the transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfer for both read and write transactions. For PCI cycles, asserted when the target is ready for data transfer. |
| **GDEVSEL**(GDEVSEL# for 4x mode) | AC11 | IO | **Device Select (PCI transactions only).** This signal is driven by the North Bridge when a PCI initiator is attempting to access main memory. It is an input when the chip is acting as PCI initiator. Not used for AGP cycles. Interpreted as active high for AGP 8x. |

# 5.2 K8N800 North Bridge - 2

### AGP Bus Interface (Continued)

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **AGP8XDT#** | Y2 | I | **AGP 8x Transfer Mode Detect.** Low indicates that the external graphics card can support 8x transfer mode |
| **GRBF**(GRBF# for 4x) | AD6 | I | **Read Buffer Full.** Indicates if the master (graphics controller) is ready to accept previously requested low priority read data. When GRBF# is asserted, the North Bridge will not return low priority read data to the graphics controller. |
| **GWBF**(GWBF# for 4x) | AC1 | I | **Write Buffer Full.** |
| **GSBA[7:0]#** (GSBA[7:0] for 4x) | (see pin list) | I | **Side Band Address.** Provides an additional bus to pass address and command information from the master (graphics controller) to the target (North Bridge). These pins are ignored until enabled. |
| **GSBSTBF**(GSBSTB for 4x), **GSBSTBS**(GSBSTB# for 4x) | AF1<br>AE1 | I | **Side Band Strobe.** Driven by the master to provide timing for GSBA[7:0]. 8x mode uses GSBSTBF (iBFirstlr strobe) and GSBSTBS (iBSecondl) strobe). These signals are interpreted as GSBSTB & GSBSTB# for AGP4x. |
| **GST[2:0]** | AB1<br>AA1<br>AA2 | O | **Status (AGP only).** Provides information from the arbiter to a master to indicate what it may do. Only valid while GGNT# is asserted.<br>000 Indicates that previously requested low priority read or flush data is being returned to the master (graphics controller).<br>001 Indicates that previously requested high priority read data is being returned to the master.<br>010 Indicates that the master is to provide low priority write data for a previously enqueued write command.<br>011 Indicates that the master is to provide high priority write data for a previously enqueued write command.<br>100 Reserved. (arbiter must not issue, may be defined in the future).<br>101 Reserved. (arbiter must not issue, may be defined in the future).<br>110 Reserved. (arbiter must not issue, may be defined in the future).<br>111 Indicates that the master (graphics controller) has been given permission to start a bus transaction. The master may enqueue AGP requests by asserting PIPE# or start a PCI transaction by asserting GFRM#. ST[2:0] are always outputs from the target (North Bridge logic) and inputs to the master (graphics controller). |

### AGP Bus Interface (Continued)

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **GSTOP**(GSTOP# for 4x) | AC12 | IO | **Stop (PCI transactions only).** Asserted by the target to request the master to stop the current transaction. Interpreted as active high for AGP 8x. |
| **GREQ**(GREQ# for 4x) | Y1 | I | **Request.** Master (graphics controller) request for use of the AGP bus. |
| **GGNT**(GGNT# for 4x) | AA3 | O | **Grant.** Permission is given to the master (graphics controller) to use the AGP bus. |
| **GSERR**(GSERR# for 4x) | AC15 | IO | **AGP System Error.** |

Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see isAdditional 12C InterfaceslÓo, and display pin description tables later in this document for more information).
Note: The AGP interface pins can be optionally configured as additional interfaces for connecting to external display devices. For simplification of the AGP pin description tables above and on the next page, that multiplexing is not shown here (see isAdditional I2C Interfacesll and display pin description tables later in this document for more information).
Note: Separate system interrupts are not provided for AGP. The AGP connector provides interrupts via PCI bus INTA-B#.
Note: A separate reset is not required for the AGP bus (RESET# resets both PCI and AGP buses)
Note: Two mechanisms are provided by the AGP bus to enqueue master requests: GPIPE# (to send addresses multiplexed on the AD lines) and the SBA port (to send addresses unmultiplexed). AGP masters implement one or the other or select one at initialization time (they are not allowed to change during runtime). Only one of the two will be used; the signals associated with the other will not be used. GRBF# has an internal pullup to maintain it in the de-asserted state in case it is not implemented on the master device. AGP 8x mode allows only SBA (GPIPE# isn™t used in 8x mode).
Note: AGP 8x signal levels are 0V and 0.8V. AGP 8x mode maintains most signals at a low level when inactive resulting in no current flow.

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## V-Link Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **VAD7,**<br>**VAD6,**<br>**VAD5**,<br>**VAD**4,<br>**VAD**3,<br>**VAD**2,<br>**VAD**1,<br>**VAD0** | AF25<br>AD24<br>AF20<br>AE19<br>AE24<br>AF24<br>AD21<br>AD20 | IO<br>IO<br>IO<br>IO<br>IO<br>IO<br>IO<br>IO | **Address / Data Bus.** Also used to pass strap information from the South Bridge to the North Bridge (the actual straps are on the indicated South Bridge pin and that information is passed to the North Bridge at reset time via the VAD pins). |
| **VPAR** | AF19 | IO | **Parity.** |
| **VBE#** | AE21 | IO | **Byte Enable.** |
| **UPCMD** | AF26 | I | **Command from Client (South Bridge) to Host (North Bridge).** |
| **UPSTB** | AE23 | I | **Strobe from Client to Host.** |
| **UPSTB#** | AF23 | I | **Complement Strobe from Client to Host.** |
| **DNCMD** | AD23 | O | **Command from Host (North Bridge) to Client (South Bridge).** |
| **DNSTB** | AF22 | O | **Strobe from Host to Client.** |
| **DNSTB#** | AD22 | O | **Complement Strobe from Host to Client.** |

## SMB / I 2 C Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **SBPLCLK** / GIRDY | AC10 | I/O | **I 2 C Serial Bus Clock for Panel (Muxed on AGP Bus Pins).** |
| **SBPLDAT** / GC#BE1 | AF11 | I/O | **I 2 C Serial Bus Data for Panel (Muxed on AGP Bus Pins).** |
| **SBDDCCLK** / GREQ | Y1 | I/O | **I 2 C Serial Bus Clock for CRT DDC (Muxed on AGP Bus Pins).** |
| **SBDDCDAT** / GGNT | AA3 | I/O | **I 2 C Serial Bus Data for CRT DDC (Muxed on AGP Bus Pins).** |
| **SPCLK[2:1]** | C2, P2 | IO | **Serial Port (SMB/I 2 C) Clocks.** Clocks for serial data transfer. SPCLK1 is typically used for I 2 C communications. SPCLK2 is typically used for CRT Display DDC communications. |
| **SPDAT[2:1]** | C1, P1 | IO | **Serial Port (SMB/I 2 C) Data.** Data signals for serial data transfer. SPDAT1 is typically used for I 2 C communications. SPDAT2 is typically used for CRT Display DDC communications. |

## Dedicated Digital Video Port 0 (DVP0) – TMDS Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **DVP0D11**/ TVD11<br>**DVP0D10**/ TVD10<br>**DVP0D9** / TVD9<br>**DVP0D8** / TVD8<br>**DVP0D7** / TVD7<br>**DVP0D6** / TVD6<br>**DVP0D5** / TVD5<br>**DVP0D4** / TVD4<br>**DVP0D3** / TVD3<br>**DVP0D2** / TVD2<br>**DVP0D1** / TVD1<br>**DVP0D0** / TVD0 | M1<br>M3<br>M2<br>L1<br>M4<br>L3<br>L2<br>K1<br>L4<br>K3<br>K2<br>J1 | O | **Digital Video Port 0 Data.** Default output drive is 8 mA. 16 mA may be selected via SR3D[6]=1.<br><br>NOTE: DVP0D[6:0] are also used for power-up reset straps for the embedded graphics controller. Check the Strap Pin table for details. |
| **DVP0HS** / TVHS | N4 | O | **Digital Video Port 0 Horizontal Sync.** Internally pulled down. |
| **DVP0VS** / TVVS | N3 | O | **Digital Video Port 0 Vertical Sync.** Internally pulled down. |
| **DVP0DE** / TVDE | N1 | O | **Digital Video Port 0 Data Enable.** Internally pulled down. |
| **DVP0DET** / TVCLKR | P4 | I | **Digital Video Port 0 Display Detect.** If VGA register 3C5.12[5]=0, 3C5.1A[5] will read 1 if display is connected. Tie to GND if not used. |
| **DVP0CLK** / TVCLK | P3 | O | **Digital Video Port 0 Clock.** Internally pulled down. |

The terminology ie3C5.nnlg above refers to the VGA iGSequencerl. registers at I/O port 3C5 index "nn"

## CRT Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **AR**<br>**AG**<br>**AB** | B3<br>A3<br>A2 | AO<br>AO<br>AO | **Analog Red.** Red output to CRT monitor.<br>**Analog Green.** Green output to CRT monitor.<br>**Analog Blue.** Blue output to CRT monitor. |
| **RSET** | C4 | AI | **CRT Output Reference Resistor.** Tie to GNDRGB through an external 90.9 ±1% resistor to control the "RGB" RAMDAC full-scale current. |
| **HSYNC** | A1 | O | **Horizontal Sync.** Digital output to CRT monitor. |
| **VSYNC** | B1 | O | **Vertical Sync.** Digital output to CRT monitor. |

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## Dedicated Digital Video Port 0 (DVP0) - TV Encoder Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **TVD11** / DVP0D11<br>**TVD10** / DVP0D10<br>**TVD9** / DVP0D9<br>**TVD8** / DVP0D8<br>**TVD7** / DVP0D7<br>**TVD6** / DVP0D6<br>**TVD5** / DVP0D5<br>**TVD4** / DVP0D4<br>**TVD3** / DVP0D3<br>**TVD2** / DVP0D2<br>**TVD1** / DVP0D1<br>**TVD0** / DVP0D0 | M1<br>M3<br>M2<br>L1<br>M4<br>L3<br>L2<br>K1<br>L4<br>K3<br>K2<br>J1 | O | **TV Encoder 0 Data.**<br><br>To configure DVP0 as a TV Out interface port, pins DVP0D[6:5] must be strapped high.<br><br>Note: One TV Encoder interface is supported through either DVP0 or GDVP1. |
| **TVHS** / DVP0HS | N4 | O | **TV Encoder 0 Horizontal Sync.** Internally pulled down. |
| **TVVS** / DVP0VS | N3 | O | **TV Encoder 0 Vertical Sync.** Internally pulled down. |
| **TVDE** / DVP0DE | N1 | O | **TV Encoder 0 Display Enable.** Internally pulled down. |
| **TVCLKR** / DVP0DET | P4 | I | **TV Encoder 0 Clock Return.** Input from TV encoder. Internally pulled down. |
| **TVCLK** / DVP0CLK | P3 | O | **TV Encoder 0 Clock Out.** Output to TV encoder. Internally pulled down. |

The above pins may be connected to an external TV Encoder chip such as a VIA VT1622A or VT1622AM for driving a TV set.
I/O pads for the pins on this page are powered by VCCGFX (3.3V I/O).

## AGP-Multiplexed Digital Video Port 1 (GDVP1) – TMDS Interface

| Signal Name | AGP Name | Pin # | I/O | Signal Description |
|---|---|---|---|---|
| **GDVP1D11** | GC#BE3 | AC7 | O | **Data.** |
| **GDVP1D10** | GD26 | AE6 | | |
| **GDVP1D9** | GD24 | AF6 | | |
| **GDVP1D8** | GD30 | AE4 | | |
| **GDVP1D7** | GD28 | AF5 | | |
| **GDVP1D6** | GD29 | AF4 | | |
| **GDVP1D5** | GSBA4# | AF2 | | |
| **GDVP1D4** | GD27 | AD5 | | |
| **GDVP1D3** | GSBA5# | AD3 | | |
| **GDVP1D2** | GSBSTBS | AE1 | | |
| **GDVP1D1** | GSBSTBF | AF1 | | |
| **GDVP1D0** | GSBA2# | AD1 | | |
| **GDVP1HS** | GSBA3# | AD2 | O | **Horizontal Sync.** |
| **GDVP1VS** | GSBA0# | AC2 | O | **Vertical Sync.** |
| **GDVP1DE** | GSBA1# | AC3 | O | **Data Enable.** |
| **GDVP1DET** | GD31 | AD4 | I | **Display Detect.** If VGA register 3C5.3E[0] = 1, 3C5.1A[4] will read 1 if a display is connected. Tie to GND if not used. |
| **GDVP1CLK** | GSBA6# | AE3 | O | **Clock.** |
| **GDVP1CLK#** | GSBA7# | AF3 | O | **Clock Complement.** |

The GDVP1 Digital Video Port is supported through multiplexing its interface signal pins with AGP pins. GDVP1 can be configured as either a TMDS transmitter interface port or a TV Encoder interface port. (see the TMDS Transmitter Interface and TV Encoder Interface pin lists below for details).

## Analog Power / Ground

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **VCCATX** | C22 | P | **Analog Power for HT Transmit.** 3.3V ±5%. Connect through a ferrite bead for isolation of digital switching noise. |
| **GNDATX** | C21 | P | **Analog Ground for HT Transmit.** Connect to main ground plane through a ferrite bead for isolation of digital switching noise. |
| **VCCARX** | E25 | P | **Analog Power for HT Receive.** 3.3V ±5%. Connect through a ferrite bead for isolation of digital switching noise. |
| **GNDARX** | E26 | P | **Analog Ground for HT Receive.** Connect to main ground plane through a ferrite bead for isolation of digital switching noise. |

## Reference Voltages

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **VLVREF** | AF21 | P | **V-Link Voltage Reference.** 0.625V ±2% derived using a resistive voltage divider (3K §Ù to 2.5V and 1K §Ù to ground). See Design Guide for details. |
| **AGPVREF[1:0]** | AC6, AC13 | P | **AGP Voltage Reference.** 0.5 VCCQQ (0.75V) for AGP 2.0 (4x transfer mode) and 0.23 VCCQQ (0.35V) for AGP 3.0 (8x transfer mode). See the Design Guide for additional information and circuit implementation details.. |

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## AGP-Multiplexed Digital Video Port 1 (GDVP1) – TV Encoder

| Signal Name | AGP Name | Pin # | I/O | Signal Description |
|---|---|---|---|---|
| **GTVD11** / GDVP1D11,<br>**GTVD10** / GDVP1D10,<br>**GTVD9** / GDVP1D9,<br>**GTVD8** / GDVP1D8,<br>**GTVD7** / GDVP1D7,<br>**GTVD6** / GDVP1D6,<br>**GTVD5** / GDVP1D5,<br>**GTVD4** / GDVP1D4,<br>**GTVD3** / GDVP1D3,<br>**GTVD2** / GDVP1D2,<br>**GTVD1** / GDVP1D1,<br>**GTVD0** / GDVP1D0 | GC#BE3<br>GD26<br>GD24<br>GD30<br>GD28<br>GD29<br>GSBA4#<br>GD27<br>GSBA5#<br>GSBSTBS<br>GSBSTBF<br>GSBA2# | AC7<br>AE6<br>AF6<br>AE4<br>AF5<br>AF4<br>AF2<br>AD5<br>AD3<br>AE1<br>AF1<br>AD1 | O | **Data.** |
| **GTVHS** / GDVP1HS | GSBA3# | AD2 | O | **Horizontal Sync.** Internally pulled down. |
| **GTVVS** / GDVP1VS | GSBA0# | AC2 | O | **Vertical Sync.** Internally pulled down. |
| **GTVDE** / GDVP1DE | GSBA1# | AC3 | O | **Display Enable.** Internally pulled down. |
| **GTVCLKR** / GDVP1DET | GD31 | AD4 | I | **Clock In.** Input from TV encoder. Internally pulled down. |
| **GTVCLK** / GDVP1CLK | GSBA6# | AE3 | O | **Clock Out.** Output to TV encoder. Internally pulled down. |
| **GTVCLK#** / GDVP1CLK# | GSBA7# | AF3 | O | **Clock Out Complement.** Output to TV encoder. Internally pulled down. |

The above pins may be connected to an external TV Encoder chip such as a VIA VT1623 or VT1623M for driving a TV set.
I/O pads for the pins on this page are powered by VCC15AGP (1.5V I/O).

## Flat Panel Power Control (Muxed with AGP)

| Signal Name | AGP Name | Pin # | I/O | Signal Description |
|---|---|---|---|---|
| **ENAVDD** | GST1 | AA1 | IO | **Enable Panel VDD Power.** |
| **ENAVEE** | GST0 | AA2 | IO | **Enable Panel VEE Power.** |
| **ENABLT** | GST2 | AB1 | IO | **Enable Panel Back Light.** |

Note: I/O pads for all pins on this page are powered by VCC15AGP (i.e., 1.5V I/O).

## 24-Bit / Dual 12-Bit Flat Panel Display Interface

| Signal Name | AGP Name | Pin # | I/O | Signal Description |
|---|---|---|---|---|
| **FPD23 / FPD0D11,**<br>**FPD22 / FPD0D10,**<br>**FPD21 / FPD0D09,**<br>**FPD20 / FPD0D08,**<br>**FPD19 / FPD0D07,**<br>**FPD18 / FPD0D06,**<br>**FPD17 / FPD0D05,**<br>**FPD16 / FPD0D04,**<br>**FPD15 / FPD0D03,**<br>**FPD14 / FPD0D02,**<br>**FPD13 / FPD0D01,**<br>**FPD12 / FPD0D00,**<br>**FPD11 / FPD1D1**1,<br>**FPD10 / FPD1D1**0,<br>**FPD09 / FPD1D0**9,<br>**FPD08 / FPD1D0**8,<br>**FPD07 / FPD1D0**7,<br>**FPD06 / FPD1D0**6,<br>**FPD05 / FPD1D0**5,<br>**FPD04 / FPD1D0**4,<br>**FPD03 / FPD1D0**3,<br>**FPD02 / FPD1D0**2,<br>**FPD01 / FPD1D0**1,<br>**FPD00 / FPD1D00** | GD11<br>GD13<br>GD14<br>GD15<br>GC#BE2<br>GD16<br>GD17<br>GD18<br>GD23<br>GD20<br>GD22<br>GADSSTB1<br>F<br>GD1<br>GD0<br>GD3<br>GD4<br>GD5<br>GD6<br>GD7<br>GADSTB0F<br>GC#BE0<br>GADSTB0S<br>GD10<br>GD12 | AE13<br>AD12<br>AF12<br>AE12<br>AD11<br>AD10<br>AE10<br>AF10<br>AD8<br>AF9<br>AE9<br>AE7<br>AD18<br>AF18<br>AF17<br>AD17<br>AD16<br>AE16<br>AF16<br>AE15<br>AD15<br>AF15<br>AD13<br>AF13 | O | **Flat Panel Data.** For 24-bit or dual 12-bit flat panel display modes.<br>Two FPD interface modes, 24-bit and dual 12-bit, are supported.<br>Strapping pin DVP0D4 is used to select the interface mode to the LVDS transmitter chip:<br>Strap High (3C5.12[4]=1): 24-bit<br>Strap Low (3C5.12[4]=0): Dual 12-bit<br>In in24-bitl] mode, only one set of control pins is required. However, in dual 12-bit mode, the K8N800 Version CD provides two sets of control signals that are required for certain LVDS transmitter chips.<br>In 24-bit mode, two operating modes are supported:<br>3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=0<br>Double data rate: each rising & falling clock edge transmits a complete 24-bit pixel<br>3C5.12[4]=1 & 3x5.88[2]=0 & 3x5.88[4]=1<br>Single data rate: each clock rising edge transmits a complete 24-bit pixel<br>In dual 12-bit mode,<br>3C5.12[4]=0 & 3x5.88[2] = 1<br>Each rising and falling clock edge transmits half (12 bits) of two 24-bit pixels |
| **FPHS** | GFRAME | AC9 | O | **Flat Panel Horizontal Sync.** 24-bit mode or port 0 of dual 12-bit mode. |
| **FPVS** | GDEVSEL | AC11 | O | **Flat Panel Vertical Sync.** 24-bit mode or port 0 of dual 12-bit mode. |
| **FPDE** | GD19 | AD9 | O | **Flat Panel Data Enable.** 24-bit mode or port 0 of dual 12-bit mode |
| **FPDET** | GADSTB1S | AF7 | I | **Flat Panel Detect.** 24-bit mode or port 0 of dual 12-bit mode |
| **FPCLK** | GD21 | AF8 | O | **Flat Panel Clock.** 24-bit mode or port 0 of dual 12-bit mode |
| **FPCLK#** | GWBF | AC1 | O | **Flat Panel Clock Complement.** 24-bit mode or port 0 of dual 12-bit<br>Mode. |

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### 24-Bit / Dual 12-Bit Flat Panel Display Interface (Continued)

| Signal Name | AGP Name | Pin # | I/O | Signal Description |
|---|---|---|---|---|
| **FP1HS** | GD9 | AD14 | O | **Flat Panel Horizontal Sync.** For port 1 in dual 12-bit mode. |
| **FP1VS** | GPAR | AC16 | O | **Flat Panel Vertical Sync.** For port 1 in dual 12-bit mode. |
| **FP1DE** | GSERR | AC15 | O | **Flat Panel Data Enable.** For port 1 in dual 12-bit mode. |
| **FP1DET** | GD8 | AF14 | I | **Flat Panel Detect.** For port 1 in dual 12-bit mode. |
| **FP1CLK** | GD2 | AE18 | O | **Flat Panel Clock.** For port 1 in dual 12-bit mode. |
| **FP1CLK#** | GSTOP | AC12 | O | **Flat Panel Clock Complement.** For port 1 in dual 12-bit mode. |

### Compensation

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **RPCOMP** | D25 | AI | **Host CPU P-Channel Compensation.** Connect 50 §Ù 1% resistor to GND. |
| **RNCOMP** | D26 | AI | **Host CPU N-Channel Compensation.** Connect 50 §Ù 1% resistor to VCCHT. |
| **RTCOMP** | C26 | AI | **Host CPU Compensation.** Connect 100 §Ù 1% resistor to VCCHT. |
| **VLPCOMP** | AD19 | AI | **V-Link P-Channel Compensation.** Connect 360 §Ù 1% resistor to ground. |
| **AGPNCOMP** | W1 | AI | **AGP N-Channel Compensation.** Connect 60.4 §Ù 1% resistor to VCCAGP. |
| **AGPPCOMP** | V1 | AI | **AGP P-Channel Compensation.** Connect 60.4 §Ù 1% resistor to GND. |

### Clock, Reset, Power Control, General Purpose I/O, Interrupts and Test

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **GCLK** | A11 | I | **AGP Clock.** 66 MHz clock for AGP logic. |
| **DCLKI** | D7 | I | **Dot Clock (Pixel Clock) In.** For spread spectrum. |
| **DCLKO** | A7 | O | **Dot Clock (Pixel Clock) Out.** For spread spectrum. |
| **RESET#** | AD25 | I | **Reset.** Input from the South Bridge chip. 3.3V tolerant input. When asserted, this signal resets the chip and sets all register bits to the default value. The rising edge of this signal is used to sample all power-up strap options In addition, HTRST# is driven active to reset the K8 CPU. |
| **PWROK** | AE26 | I | **Power OK.** Driven by South Bridge PWROK output from the power supply PWRGOOD input to the South Bridge. |
| **SUSST#** | AD26 | I | **Suspend Status.** For implementation of the Suspend-to-DRAM feature. Connect to an external pull-up to disable. |
| **TESTIN** | AC26 | I | **Test In.** This pin is used for testing and must be left unconnected or tied high (4.7K §Ù to 2.5V) on all board designs. |
| **BISTIN** | D3 | I | **Built-In-Self-Test In.** Reserved for test. Connect to GND for normal operation. |
| **DEBUG** | AC17 | I | **Debug.** Reserved for test. Connect to ground for normal operation. |
| **XIN** | C6 | I | **Reference Frequency In.** 14.31818 MHz. |
| **INTA#** | E7 | O | **PCI Interrupt Output A.** Connect to the South Bridge. |
| **GPOUT** | D2 | O | **General Purpose Output.** |
| **GPO0** | N2 | O | **General Purpose Output.** |

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### Integrated Graphics Power and Ground

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **VCCDAC** | B2 | P | **DAC Voltage.** 3.3V ±5% connected via ferrite bead for isolation of digital switching noise. |
| **GNDDAC** | C3, D4 | P | **DAC Ground.** Connect to main ground plane. |
| **VCCRGB** | A4 | P | **Power for CRT RGB Outputs.** 3.3V ±5% connected via ferrite bead for isolation of digital switching noise |
| **GNDRGB** | B4 | P | **Connection point for RGB Load Resistors.** Connect to main ground plane via ferrite bead for isolation of digital switching noise. |
| **VCCPLL1** | D5 | P | **Power for Graphics Controller PLL1 (“E-Clock”).** 1.5V ±5% connected via ferrite bead for isolation of digital switching noise. |
| **GNDPLL1** | C5 | P | **Ground for Graphics Controller PLL1 (“E-Clock”).** Connect to main ground plane via ferrite bead for isolation of digital switching noise. |
| **VCCPLL2** | A5 | P | **Power for Graphics Controller PLL2 (“D-Clock”).** 1.5V ±5% connected via ferrite bead for isolation of digital switching noise. |
| **GNDPLL2** | B5 | P | **Ground for Graphics Controller PLL2 (“D-Clock”).** Connect to main ground plane via ferrite bead for isolation of digital switching noise. |
| **VCCPLL3** | A6 | P | **Power for Graphics Controller PLL3 (“LCD Clock”).** 1.5V ±5% connected via ferrite bead for isolation of digital switching noise. |
| **GNDPLL3** | B6 | P | **Ground for Graphics Controller PLL3 (“LCD Clock”).** Connect to main ground plane via ferrite bead for isolation of digital switching noise. |

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### V-Link Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **VD[7:0]** | (see pin list) | IO | **Data Bus.** These pins are also used to send strap information to the chipset north bridge. At power up, VD7 reflects the state of a strap on SDCS3#, VD[6:4] reflect the state of straps on pins SDA[2:0], and VD[3:0] reflect the state of straps on pins Strap_VD3-0. The specific interpretation of these straps is north bridge chip design dependent. |
| VPAR | F24 | IO | **Parity.** If the VPAR function is implemented in a compatible manner on the north bridge, this pin should be connected to the north bridge VPAR pin (P4X333, P4X400, P4X800, KT400). If VPAR is not implemented in the north bridge chip or is incompatible with the 8235CE (4x V-Link north bridges) connect this pin to an 8.2K pullup to 2.5V (Pro266, Pro266T, KT266, KT266A, KT333, P4X266, PN266, KN266, KM266, P4M266, P4N266). See app note AN222 for details. |
| **VBE#** | G24 | IO | **Byte Enable.** |
| **VCLK** | L22 | I | **V-Link Clock.** |
| **UPCMD** | K23 | O | **Command from Client-to-Host.** |
| **DNCMD** | K25 | I | **Command from Host-to-Client.** |
| **UPSTB** | J26 | O | **Strobe from Client-to-Host.** |
| **UPSTB#** | J24 | O | **Complement Strobe from Client-to-Host.** |
| **DNSTB** | K26 | I | **Strobe from Host-to-Client.** |
| **DNSTB#** | H24 | I | **Complement Strobe from Host-to-Client.** |

### CPU Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **A20M#** | U26 | OD | **A20 Mask.** Connect to A20 mask input of the CPU to control address bit-20 generation. Logical combination of the A20GATE input (from internal or external keyboard controller) and Port 92 bit-1 (Fast_A20). |
| FERR# | U24 | I | **Numerical Coprocessor Error.** This signal is tied to the coprocessor error signal on the CPU. Internally generates interrupt 13 if active. Output voltage swing is programmable tot 1.5V or 2.5V by Device 17 Function 0 Rx67[2]. |
| **IGNNE#** | T24 | OD | **Ignore Numeric Error.** This pin is connected to the CPU iPignore errorlr pin. |
| **INIT#** | R26 | OD | **Initialization.** The VT8235 Version CE asserts INIT# if it detects a shut-down special cycle on the PCI bus or if a soft reset is initiated by the register |
| **INTR** | T25 | OD | **CPU Interrupt.** INTR is driven by the VT8235 Version CE to signal the CPU that an interrupt request is pending and needs service. |
| **NMI** | T26 | OD | **Non-Maskable Interrupt.** NMI is used to force a non-maskable interrupt to the CPU. The VT8235 Version CE generates an NMI when PCI bus SERR# is asserted. |
| **SLP#** | V26 | OD | **Sleep.** Used to put the CPU to sleep. |
| **SMI#** | U25 | OD | **System Management Interrupt.** SMI# is asserted by the VT8235 Version CE to the CPU in response to different Power-Management events. |
| **STPCLK#** | R24 | OD | **Stop Clock.** STPCLK# is asserted by the VT8235 Version CE to the CPU to throttle the processor clock. |

Note: Connect each of the above signals to 150 §Ù pullup resistors to VCC_CMOS (see Design Guide).

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### Advanced Programmable Interrupt Controller (APIC) Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **APICD1** | T23 | O | **Internal APIC Data 1.** Function 0 Rx58[6] = 1 |
| APICD0 | R25 | O | **Internal APIC Data 0.** Function 0 Rx58[6] = 1 |
| **APICCLK** | U23 | I | **APIC Clock.** |

### CPU Speed Control Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **VRDSLP** / GPI29/ GPO29 | AB9 | OD | **Voltage Regulator Deep Sleep.** Connected to the CPU voltage regulator. High selectsthe proper voltage for deep sleep mode. This pin performs the VRDPSLP function if Function 0 RxE5[3] = 0. |
| GHI# / **GPI22/ GPO22** | R22 | OD | **CPU Speed Select.** Connected to the CPU voltage regulator, used to select high speed (L) or low speed (H). This pin performs the GHI# function if Function 0 RxE5[3] = 0. |
| **DPSLP#** / GPI23/ GPO23 | P21 | OD | **CPU Deep Sleep.** This pin performs the DPSLP# function if Device 17 Function 0RxE5[3]=0. |
| **CPUMISS** / GPI17 | Y1 | I | **CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time. |
| **AGPBZ#** / GPI6 | AD10 | I | **AGP Busy.** Low indicates that an AGP master cycle is in progress (CPU speed transitions will be postponed if this input is asserted low). Connected to the AGP Bus AGPBZ# pin. |

### PCI Bus Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **AD[31:0]** | (see pinlist) | IO | **Address / Data Bus.** Multiplexed address and data. The address is driven with FRAME#assertion and data is driven or received in following cycles. |
| CBE[3:0]# | M3, L4, C1, E2 | IO | **Command / Byte Enable.** The command is driven with FRAME# assertion. Byteenables corresponding to supplied or requested data are driven on following clocks. |
| **DEVSEL#** | H2 | IO | **Device Select.** The VT8235 Version CE asserts this signal to claim PCI transactions through positive or subtractive decoding. As an input, DEVSEL# indicates the response to a VT8235 Version CE-initiated transaction and is also sampled when decoding whether to subtractively decode the cycle. |
| **FRAME#** | J1 | IO | **Frame.** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator. |
| **IRDY#** | J2 | IO | **Initiator Ready.** Asserted when the initiator is ready for data transfer. |
| **TRDY#** | H1 | IO | **Target Ready.** Asserted when the target is ready for data transfer. |
| **STOP#** | K4 | IO | **Stop.** Asserted by the target to request the master to stop the current transaction. |
| **SERR#** | C2 | I | **System Error.** SERR# can be pulsed active by any PCI device that detects a system error condition. Upon sampling SERR# active, the VT8235 Version CE can be programmed to generate an NMI to the CPU. |
| **PERR#** | C3 | _ | **Parity Error.** PERR#, sustained tri-state, is only for the reporting of data parity errors during all PCI transactions except for a Special Cycle. |
| **PAR** | F4 | IO | **Parity.** A single parity bit is provided over AD[31:0] and C/BE[3:0]#. |

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## PCI Bus Interface (Continued)

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **INTA#**<br>**INTB#**<br>**INTC#**<br>**INTD#**<br>**INTE#** / GPI12, / GPO12,<br>**INTF#** / GPI13, / GPO13,<br>**INTG#** / GPI14, / GPO14,<br>**INTH#** / GPI15, / GPO15 | A4<br>B4<br>B5<br>C4<br>D4<br>E4<br>A3<br>B3 | I | **PCI Interrupt Reques**t. The INTA# through INTD# pins are typically connected to thePCI bus INTA#-INTD# pins per the table below. INTE-H# are enabled by setting Device17, Function 0 Rx5B[1] = 1. BIOS settings must match the physical connection method.<br>INTA# INTB# INTC# INTD#<br>PCI Slot 1 INTA# NTB# INTC# INTD#<br>PCI Slot 2 INTB# INTC# INTD# INTE#<br>PCI Slot 3 INTC# INTD# INTE# INTF#<br>PCI Slot 4 INTD# INTE# INTF# INTG#<br>PCI Slot 5 INTE# INTF# INTG# INTH#<br>PCI Slot 6 INTF# INTG# INTH# INTA# |
| **REQ5#** / GPI7,<br>**REQ4#,**<br>**REQ3#,**<br>**REQ2#,**<br>**REQ1#,**<br>**REQ0#** | R3<br>P3<br>D5<br>C5<br>B6<br>A5 | I | **PCI Request.** These signals connect to the VT8235 Version CE from each PCI slot (oreach PCI master) to request the PCI bus. To use pin R3 as REQ5#, Function 0 RxE4 mustbe set to 1 otherwise this pin will function as General Purpose Input 7. |
| **GNT5#** / GPO7,<br>**GNT4#,**<br>**GNT3#,**<br>**GNT2#,**<br>**GNT1#,**<br>**GNT0#** | R2<br>R4<br>E5<br>C6<br>D6<br>A6 | O | **PCI Grant.** These signals are driven by the VT8235 Version CE to grant PCI access to aspecific PCI master. To use pin R2 as GNT5#, Function 0 RxE4 must be set to 1otherwise this pin will function as General Purpose Output 7. |
| **PCIRST#** | R1 | O | **PCI Reset.** This signal is used to reset devices attached to the PCI bus. |
| **PCICLK** | R23 | I | **PCI Clock.** This signal provides timing for all transactions on the PCI Bus. |
| **PCKRUN#** | AB7 | IO | **PCI Bus Clock Run.** This signal indicates whether the PCI clock is or will be stopped (high) or running (low). The VT8235 Version CE drives this signal low when the PCI clock is running (default on reset) and releases it when it stops the PCI clock. External devices may assert this signal low to request that the PCI clock be restarted or prevent it from stopping. Connect this pin to ground using a 100 §Ù resistor if the function is not used. Refer to the ihPCI Mobile Design Guidelo and applicable VIA North Bridge Design Guide (KT400A, CLE266, or P4X400) for more details. |

## LAN Controller - Media Independent Interface (MII)

| Signal Name | Pin # | I/O | PU | Signal Description |
|---|---|---|---|---|
| **MCOL** | B11 | I | ***PD*** | **MII Collision Detect.** From the external PHY. |
| **MCRS** | A11 | I | ***PD*** | **MII Carrier Sense.** Asserted by the external PHY when the media is active. |
| **MDCK** | A7 | O | ***PD*** | **MII Management Data Clock.** Sent to the external PHY as a timing reference for MDIO |
| **MDIO** | B7 | IO | ***PD*** | **MII Management Data I/O.** Read from the MDI bit or written to the MDO bit. |
| **MRXCLK** | C9 | I | ***PD*** | **MII Receive Clock.** 2.5 or 25 MHz clock recovered by the PHY. |
| **MRXD[3-0]** | C7, A8, B8, C8 | I | ***PD*** | **MII Receive Data.** Parallel receive data lines driven by the external PHY synchronous with MRXCLK. |
| **MRXDV** | D8 | I | ***PD*** | **MII Receive Data Valid.** |
| **MRXERR** | D10 | I | ***PD*** | **MII Receive Error.** Asserted by the PHY when it detects a data decoding error. |
| **MTXCLK** | C10 | I | ***PD*** | **MII Transmit Clock.** Always active 2.5 or 25 MHz clock supplied by the PHY. |
| **MTXD[3-0]** | A9, B9, B10, A10 | O | ***PD*** | **MII Transmit Data.** Parallel transmit data lines synchronized to MTXCLK. |
| **MTXENA** | C11 | O | ***PD*** | **MII Transmit Enable.** Signals that transmit is active from the MII port to the PHY. |
| **MIIVCC** | D9, E9, E10, E11 | **Power** | | **MII Interface Power.** 3.3V ±5%. |
| **MIIVCC25** | D12, E12 | **Power** | | **MII Suspend Power.** 2.5V ±5%. |
| **RAMVCC** | E7 | **Power** | | **Power For Internal LAN RAM.** 2.5V ±5%. |
| **RAMGND** | E6 | **Power** | | **Ground For Internal LAN RAM.** |

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### Serial EEPROM Interface

| Signal Name | Pin # | I/O | PU | Signal Description |
|---|---|---|---|---|
| **EECS#** | **D11** | **O** | | Serial EEPROM Chip Select. |
| **EECK** | **C12** | **O** | | Serial EEPROM Clock. |
| **EEDO** | **B12** | **I** | | Serial EEPROM Data Output. **Connect to EEPROM Data Out pin.** |
| **EEDI** | **A12** | **O** | | Serial EEPROM Data Input. **Connect to EEPROM Data In pin.** |

### Low Pin Count (LPC) Interface

| Signal Name | Pin # | I/O | PU | Signal Description |
|---|---|---|---|---|
| **LFRM#** | **AF6** | **IO** | | LPC Frame. |
| **LREQ#** | **AE6** | **IO** | | LPC DMA / Bus Master Request. |
| **LAD[3-0]** | **AD7, AE7, AF7, AD8** | **IO** | **PU** | LPC Address / Data. |

Note: Connect the LPC interface LPCRST# (LPC Reset) signal to PCIRST#

### System Management Bus (SMB) Interface (I 2 C Bus)

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **SMBCK1** | AC4 | IO | **SMB / I 2 C Channel 1 Clock.** |
| **SMBCK2** / GPI27 / GPO27 | AC3 | IO | **SMB / I 2 C Channel 2 Clock.** Rx95[2] = 0 |
| **SMBDT1** | AB2 | IO | **SMB / I 2 C Channel 1 Data.** |
| **SMBDT2** / GPI26 / GPO26 | AD1 | IO | **SMB / I 2 C Channel 2 Data.** Rx95[2] = 0 |
| **SMBALRT#** | AB1 | I | **SMB Alert.** (enabled by System Management Bus I/O space Rx08[3] =<br>1) When the chip is enabled to allow it, assertion generates an IRQ or<br>SMI interrupt or a power management resume event. Connect to a 10K<br>ohm pullup to VSUS33 if not used. |

### Universal Serial Bus 2.0 Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **USBP0+** | E20 | IO | **USB 2.0 Port 0 Data +** |
| USBP0Œ | D20 | IO | **USB 2.0 Port 0 Data Œ** |
| USBP1+ | A20 | IO | **USB 2.0 Port 1 Data +** |
| USBP1Œ | B20 | IO | **USB 2.0 Port 1 Data Œ** |
| USBP2+ | E18 | IO | **USB 2.0 Port 2 Data +** |
| USBP2Œ | D18 | IO | **USB 2.0 Port 2 Data Œ** |
| USBP3+ | A18 | IO | **USB 2.0 Port 3 Data +** |
| USBP3Œ | B18 | IO | **USB 2.0 Port 3 Data Œ** |
| USBP4+ | D16 | IO | **USB 2.0 Port 4 Data +** |
| USBP4Œ | E16 | IO | **USB 2.0 Port 4 Data Œ** |
| USBP5+ | A16 | IO | **USB 2.0 Port 5 Data +** |
| USBP5Œ | B16 | IO | **USB 2.0 Port 5 Data Œ** |
| USBCLK | E23 | I | **USB 2.0 Clock.** 48MHz clock input for the USB interface |
| USBOC0# | C26 | I | **USB 2.0 Port 0 Over Current Detect.** Port 0 is disabled if low. |
| USBOC1# | D24 | I | **USB 2.0 Port 1 Over Current Detect.** Port 1 is disabled if low. |
| USBOC2# | B26 | I | **USB 2.0 Port 2 Over Current Detect.** Port 2 is disabled if low. |
| USBOC3# | C25 | I | **USB 2.0 Port 3 Over Current Detect.** Port 3 is disabled if low. |
| USBOC4# | B24 | I | **USB 2.0 Port 4 Over Current Detect.** Port 4 is disabled if low. |
| USBOC5# | A24 | I | **USB 2.0 Port 5 Over Current Detect.** Port 5 is disabled if low. |
| USBVCC | (see pin list) | **Power** | **USB 2.0 Port Differential Output Interface Logic Voltage.** 3.3V |
| USBGND | (see pin list) | **Power** | **USB 2.0 Port Differential Output Interface Logic Ground.** |
| VSUSUSB | C24 | **Power** | **USB 2.0 Suspend Power.** 2.5V ±5%. |
| VCCUPLL | A23, B23 | **Power** | **USB 2.0 PLL Analog Voltage.** 2.5V ±5%. |
| GNDUPLL | C23, D23 | **Power** | **USB 2.0 PLL Analog Ground.** |

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### UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **PDRDY** /PDDMARDY /PDSTROBE | Y22 | I | EIDE Mode: **Primary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Primary Device DMA Read**y. Output flow control. The device mayassert DDMARDY to pause output transfers **Primary Device Strob**e. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers |
| **SDRDY** /SDDMARDY /SDSTROBE | AF17 | I | EIDE Mode: **Secondary I/O Channel Ready.** Device ready indicator UltraDMA Mode: **Secondary Device DMA Read**y. Output flow control. The devicemay assert DDMARDY to pause output transfers **Secondary Device Strob**e. Input data strobe (both edges). The device may stop DSTROBE to pause input data transfers |
| **PDIOR#** /PHDMARDY /PHSTROBE | W26 | O | EIDE Mode: **Primary Device I/O Read.** Device read strobe UltraDMA Mode: **Primary Host DMA Read**y. Primary channel input flow contro**l.** Thehost may assert HDMARDY to pause input transfers **Primary Host Strob**e. Output data strobe (both edges). The host may stop HSTROBE to pause output data transfers |
| **SDIOR#** /SHDMARDY /SHSTROBE | AF23 | O | EIDE Mode: **Secondary Device I/O Read.** Device read strobe UltraDMA Mode: **Secondary Host DMA Read**y. Input flow control. The host mayassert HDMARDY to pause input transfers **Host Strobe** B. Output strobe (both edges). The host may stop HSTROBE to pause output data transfers |
| **PDIOW#** /PSTOP | Y25 | O | EIDE Mode: **Primary Device I/O Write.** Device write strobe UltraDMA Mode: **Primary Sto**p. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst. |
| **SDIOW#** /SSTOP | AE23 | O | EIDE Mode: **Secondary Device I/O Write.** Device write strobe UltraDMA Mode: **Secondary Sto**p. Stop transfer: Asserted by the host prior to initiation of an UltraDMA burst; negated by the host before data is transferred in an UltraDMA burst. Assertion of STOP by the host during or after data transfer in UltraDMA mode signals the termination of the burst. |
| **PDDRQ** | Y23 | I | **Primary Device DMA Request.** Primary channel DMA request |
| **SDDRQ** | AD17 | I | **Secondary Device DMA Request.** Secondary channel DMA request |

### UltraDMA-133 / 100 / 66 / 33 Enhanced IDE Interface (Continued)

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **PDDACK#** | Y24 | O | **Primary Device DMA Acknowledge.** Primary channel DMA acknowledge |
| **SDDACK#** | AD23 | O | **Secondary Device DMA Acknowledge.** Secondary channel DMA acknowledge |
| **IRQ14** | AD24 | I | **Primary Channel Interrupt Request.** |
| **IRQ15** | AE26 | I | **Secondary Channel Interrupt Request.** |
| **PDCS1#** | V22 | O | **Primary Master Chip Select.** This signal corresponds to CS1FX# on the primary IDE connector. |
| **PDCS3#** | V23 | O | **Primary Slave Chip Select.** This signal corresponds to CS3FX# on the primary IDE connector. |
| **SDCS1#** / strap | AF25 | O | **Secondary Master Chip Select.** This signal corresponds to CS17X# on the secondary IDE connector. Strap low (resistor to ground) to enable serial EEPROM interface via the MII bus (this disables the EExx pins). This pin has an internal pullup to default to serial EEPROM interface via the EExx pins. |
| **SDCS3#** / strap | AF26 | O | **Secondary Slave Chip Select.** This signal corresponds to CS37X# on the secondary IDE connector. Strap information is communicated to the north bridge via VD[7]. |
| **PDA[2-0]** | W24, V25, W23 | O | **Primary Disk Address.** PDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed. |
| **SDA[2-0]** / strap | AE24, AC22, AF24 | O | **Secondary Disk Address.** SDA[2:0] are used to indicate which byte in either the ATA command block or control block is being accessed. Strap information is communicated to the north bridge via VD[6:4]. |
| **PDD[15-0]** | (see pin list) | IO | **Primary Disk Data.** |
| **SDD[15-0]** | (see pin list) | IO | **Secondary Disk Data.** |

### Serial IRQ

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **SERIRQ** | AD9 | I | **Serial IRQ.** This pin has an internal pull-up resistor. |

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### AC97 Audio / Modem Interface

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **ACRST#** | T3 | O | **AC97 Reset.** |
| **ACBTCK** | T1 | I | **AC97 Bit Clock.** |
| **ACSYNC** | T2 | O | **AC97 Sync.** |
| **ACSDO** | U2 | O | **AC97 Serial Data Out.** |
| **ACSDIN0** (VSUS33)*f* | U3 | I | **AC97 Serial Data In 0.** |
| **ACSDIN1** (VSUS33)*f* | V2 | I | **AC97 Serial Data In 1.** |
| **ACSDIN2** / GPIO20 / PCS0# | U1 | I | **AC97 Serial Data In 2.** RxE4[6]=0,E5[1]=0, PMIO Rx4C[20]=1 |
| **ACSDIN3** / GPIO21 / PCS1# / SLPBTN# | V3 | I | **AC97 Serial Data In 3.** RxE4[6]=0,E5[2]=0, PMIO Rx4C[21]=1 |

### Resets, Clocks, and Power Status

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **PWRGD** | **AC5** | **I** | **Power Good.** Connected to the Power Good signal on the Power Supply. Internal logic **powered by VBAT.** |
| **PWROK#** | **AF1** | **O** | **Power OK.** Internal logic powered by VSUS33. |
| **PCIRST#** | **R1** | **O** | **PCI Reset.** Active low reset signal for the PCI bus. The VT8235 Version CE will assert this pin during power-up or from the control register. |
| **OSC** | **AB8** | **I** | **Oscillator.** 14.31818 MHz clock signal used by the internal Timer. |
| **RTCX1** | **AE4** | **I** | **RTC Crystal Input**: 32.768 KHz crystal or oscillator input. This input is used for the internal RTC and power-well power management logic and is powered by VBAT. |
| **RTCX2** | **AF3** | **O** | **RTC Crystal Output**: 32.768 KHz crystal output. Internal logic powered by VBAT. |
| **TEST** | **AE9** | **I** | **Test.** |
| **TPO** | **AF9** | **O** | **Test Pin Output.** Output pin for test mode. |
| **NC** | **(see pin list)** | **–** | **No Connect.** Do not connect. |

### Internal Keyboard Controller

| Signal Name | Pin # | I/O | PU | Signal Description |
|---|---|---|---|---|
| **MSCK** / IRQ1 | **W1** | **IO / I** | **PU** | **MultiFunction Pin** (Internal mouse controller enabled by Rx51[1])<br>Rx51[2]=1 **Mouse Clock.** From internal mouse controller.<br>**Rx51[2]=0** Interrupt Request **1. Interrupt input 1.** |
| **MSDT** / IRQ12 | **W2** | **IO / I** | **PU** | **MultiFunction Pin** (Internal mouse controller enabled by Rx51[1])<br>Rx51[2]=1 **Mouse Data.** From internal mouse controller.<br>Rx51[2]=0 **Interrupt Request 1**2. Interrupt input 12. |
| **KBCK** / KA20G | **W3** | **IO / I** | **PU** | **MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0])<br>Rx51[0]=1 **Keyboard Clock.** From internal keyboard controller<br>Rx51[0]=0 **Gate A20.** Input from external keyboard controller. |
| **KBDT** / KBRC | **V1** | **IO / I** | **PU** | **MultiFunction Pin** (Internal keyboard controller enabled by Rx51[0])<br>Rx51[0]=1 **Keyboard Data.** From internal keyboard controller.<br>Rx51[0]=0 **Keyboard Reset.** From external keyboard controller<br>(KBC) for CPURST# generation |
| **KBCS#** / strap | **AF10** | **O** | | **Keyboard Chip Select** (Rx51[0]=0). To external keyboard controller chip. Strap high to enable LPC BIOS ROM. |

Note: KBCK, KBDT, MSCK, and MSDT are powered by the VSUS33 suspend voltage plane.

### Speaker

| Signal Name | Pin # | I/O | PU | Signal Description |
|---|---|---|---|---|
| **SPKR** / strap | **AF8** | **O** | | **Speaker.** Strap low to enable (high to disable) CPU frequency **strapping.** |

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## General Purpose Inputs

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **GPI0** ***(VBAT)*** | **AE2** | **I** | General Purpose Input 0. **Status on PMIO Rx20[0]** |
| **GPI1** ***(VSUS33)*** | **AC2** | **I** | General Purpose Input 1. **Status on PMIO Rx20[1]** |
| **GPI2** / EXTSMI# ***(VSUS33)*** | **AA1** | **I** | General Purpose Input 2. **Status on PMIO Rx20[4]** |
| **GPI3** / RING# ***(VSUS33)*** | **Y2** | **I** | General Purpose Input 3. **Status on PMIO Rx20[8]** |
| **GPI4** / LID# ***(VSUS33)*** | **AC1** | **I** | General Purpose Input 4. **Status on PMIO Rx20[11]** |
| **GPI5** / BATLOW# ***(VSUS33)*** | **V4** | **I** | General Purpose Input 5. **Status on PMIO Rx20[12]** |
| **GPI6** / AGPBZ# | **AD10** | **I** | General Purpose Input 6. **Status on PMIO Rx20[5]** |
| **GPI7** / REQ5# | **R3** | **I** | General Purpose Input 7. **RxE4[2] = 0** |
| **GPI12** / GPO12 / INTE# | **D4** | **I** | General Purpose Input 12. **RxE4[4] = 0, 5B[1]=0** |
| **GPI13** / GPO13 / INTF# | **E4** | **I** | General Purpose Input 13. **RxE4[4] = 0, 5B[1]=0** |
| **GPI14** / GPO14 / INTG# | **A3** | **I** | General Purpose Input 14. **RxE4[4] = 0, 5B[1]=0** |
| **GPI15** / GPO15 / INTH# | **B3** | **I** | General Purpose Input 15. **RxE4[4] = 0, 5B[1]=0** |
| **GPI16** / INTRUDER# ***(VBAT)*** | **AE1** | **I** | General Purpose Input 16. **Status on PMIO Rx20[6]** |
| **GPI17** / CPUMISS | **Y1** | **I** | General Purpose Input 17. **Status on PMIO Rx20[5]** |
| **GPI18** / THRM# / AOLGPI | **Y4** | **I** | General Purpose Input 18. **Rx8C[3] = 0** |
| **GPI20** / GPO20 / ACSDIN2 / PCS0# | **U1** | **I** | **General Purpose Input 20.** RxE4[6]=1, E5[1]=0, **PMIO 4C[20] = 1** |
| **GPI21** / GPO21 / ACSDIN3 / PCS1# / SLPBTN# | **V3** | **I** | **General Purpose Input 21.** RxE4[6]=1, E5[2]=0 PMIO 4C[21] = 1 |
| **GPI22** / GPO22 / GHI# | **R22** | **I** | **General Purpose Input 22.** RxE5[3] = 1, PMIO 4C[22] = 1 |
| **GPI23** / GPO23 / DPSLP# | **P21** | **I** | **General Purpose Input 23.** RxE5[3] = 1, PMIO 4C[23] = 1 |

## General Purpose Inputs (Continued)

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **GPI26** / GPO26 / SMBDT2 ***(VSUS33)*** | **AD1** | **I** | **General Purpose Input 26.** Rx95[2] = 1, 95[3] = 0 |
| **GPI27** / GPO27 / SMBCK2 ***(VSUS33)*** | **AC3** | **I** | **General Purpose Input 27.** Rx95[2] = 1, 95[3] = 0 |
| **GPI28** / GPO28 | **AC8** | **I** | **General Purpose Input 28.** RxE5[3] = 1, PMIO 4C[28] = 1 |
| **GPI29** / GPO29 / VRDSLP | **AB9** | **I** | **General Purpose Input 29.** RxE5[3] = 1, PMIO 4C[29] = 1 |

Note: Register references above are Device 17 Function 0 unless indicated otherwise.
Note: Default pin function is underlined in the signal name column above.
Note: Input pin status for the above GPI pins 31-0 is also available on PMIO Rx4B-48[31-0]
Note: See also Power Management I/O register Rx50 for input pin change status for GPI16-19 and 24-27
Note: See also Power Management I/O register Rx52 for SCI/SMI select for GPI16-19 and 24-27
Note: See also Power Management I/O register Rx4C. General purpose input pins 20-31 are shared with OD (open drain) general

## Programmable Chip Selects

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **PCS0#** / GPIO20 / ACSDIN2 | **U1** | **O** | Programmable Chip Select 0. **RxE4[6]=1, E5[1]=1** |
| **PCS1#** / GPIO21 / ACSDIN3 / SLPBTN# | **V3** | **O** | Programmable Chip Select 1. **RxE4[6]=1, E5[2]=1** |

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### General Purpose Outputs

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **GPO0** ***(VSUS33)*** | **AA3** | **O** | General Purpose Output 0. |
| **GPO1** / SUSA# ***(VSUS33)*** | **AA2** | **O** | General Purpose Output 1. **Rx94[2] = 1** |
| **GPO2** / SUSB# ***(VSUS33)*** | **AD3** | **O** | General Purpose Output 2. **Rx94[3] = 1** |
| **GPO3** / SUSST1# ***(VSUS33)*** | **Y3** | **O** | General Purpose Output 3. **Rx94[4] = 1** |
| **GPO4** / SUSCLK ***(VSUS33)*** | **AB3** | **O** | General Purpose Output 4. **Rx95[1] = 1** |
| **GPO5** / CPUSTP# | **AC7** | **O** | General Purpose Output 5. **RxE4[0] = 1** |
| **GPO6** / PCISTP# | **AD6** | **O** | General Purpose Output 6. **RxE4[1] = 1** |
| **GPO7** / GNT5# | **R2** | **O** | General Purpose Output 7. **RxE4[2] = 0** |
| **GPO12** / GPI12 / INTE# | **D4** | **O** | General Purpose Output 12. **RxE4[4]=1, 5B[1]=0** |
| **GPO13** / GPI13 / INTF# | **E4** | **O** | General Purpose Output 13. **RxE4[4]=1, 5B[1]=0** |
| **GPO14** / GPI14 / INTG# | **A3** | **O** | General Purpose Output 14. **RxE4[4]=1, 5B[1]=0** |
| **GPO15** / GPI15 / INTH# | **B3** | **O** | General Purpose Output 15. **RxE4[4]=1, 5B[1]=0** |
| **GPO20** / GPI20 / ACSDIN2 / PCS0# | **U1** | **OD** | General Purpose Output 20. **RxE4[6]=1, E5[1]=0** |
| **GPO21** / GPI21 / ACSDIN3 / PCS1# /SLPBTN# | **V3** | **OD** | General Purpose Output 21. **RxE4[6]=1, E5[2]=0** |
| **GPO22** / GPI22 / GHI# | **R22** | **OD** | General Purpose Output 22. **RxE5[3]=1, PMIO 4C[22]=1** |
| **GPO23** / GPI23 / DPSLP# | **P21** | **OD** | General Purpose Output 23. **RxE5[3]=1, PMIO 4C[23]=1** |
| **GPO26** / GPI26 / SMBDT2 ***(VSUS33ƒ)*** | **AD1** | **OD** | General Purpose Output 26. **Rx95[2] = 1, 95[3] = 1** |
| **GPO27** / GPI27 / SMBCK2 ***(VSUS33ƒ)*** | **AC3** | **OD** | General Purpose Output 27. **Rx95[2] = 1, 95[3] = 1** |

### General Purpose Outputs (Continued)

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **GPO28** / GPI28 | **AC8** | **OD** | General Purpose Output 28. **RxE5[3] = 1, PMIO 4C[28]=1** |
| **GPO29** / GPI29 / VRDSLP | **AB9** | **OD** | General Purpose Output 29. **RxE5[3] = 1, PMIO 4C[29]=1** |

Note: The output state for each of the above general purpose outputs is selectable via Power Management I/O registers Rx4C-48
Note: Default pin functions are underlined in the table above.

### Power Management and Event Detection

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **PWRBTN#** | **AD2** | **I** | **Power Button.** Used by the Power Management subsystem to monitor an external **system on/off button or switch. Internal logic powered by VSUS33.** |
| **SLPBTN#** / GPIO21/ ACSDIN3 / PCS1# | **V3** | **I** | **Sleep Button.** Used by the Power Management subsystem to monitor an external sleepbutton or switch. RxE4[6] = 1, 80[6] = 1, E5[2] = 0 and PMIO Rx4C[21] = 1 |
| **RSMRST#** | **AD4** | **I** | **Resume Reset.** Resets the internal logic connected to the VSUS33 power plane and also resets portions of the internal RTC logic. Internal logic powered by VBAT. |
| **EXTSMI#** / GPI2 | **AA1** | **IOD** | **External System Management Interrupt.** When enabled to allow it, a falling edge on this input causes an SMI# to be generated to the CPU to enter SMI mode. (10K PU to VSUS33 if not used) (3.3V only) |
| **PME#** | **W4** | **I** | **Power Management Event.** (10K PU to VSUS33 if not used) |
| **SMBALRT#** | **AB1** | **I** | **SMB Aler**t. When programmed to allow it (SMB I/O Rx8[3]=1), assertion generates an IRQ, SMI, or power management event. (10K PU to VSUS33 if not used) |

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### Power Management and Event Detection (Continued)

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **LID#** / GPI4 | **AC1** | **I** | **Notebook Computer Display Lid Open / Closed Monitor.** Used by the Power Management subsystem to monitor the opening and closing of the display lid of notebook computers. Can be used to detect either low-to-high or high-to-low transitions to generate an SMI#. (10K PU to VSUS33 if not used) |
| **INTRUDER#** / GPI16 | **AE1** | **I** | **Intrusion Indicator.** The value of this bit may be read at PMIO Rx20[6] |
| **THRM#** / GPI18/ AOLGPI | **Y4** | **I** | **Thermal Alarm Monitor.** Rx8C[3] = 1. Rising or falling edges (selectable by PMIORx2C[6]) may be detected to set status at PMIO Rx20[10]. Setting of this status bit may then be used to generate an SCI or SMI. THRM# may also be used to enable duty cycle control of stop-clock (STPCLK#) to automatically limit maximum temperature (see Device 17 Function 0 Rx8C[7-4]). |
| **RING#** / GPI3 | **Y2** | **I** | **Ring Indicator.** May be connected to external modem circuitry to allow the system to be re-activated by a received phone call. (10K PU to VSUS33 if not used) |
| **BATLOW#** / GPI5 | **V4** | **I** | **Battery Low Indicator.** (10K PU to VSUS33 if not used) (3.3V only) |
| **CPUSTP#** / GPO5 | **AC7** | **O** | **CPU Clock Stop** (RxE4[0] = 0). Signals the system clock generator to disable the CPU clock outputs. Not connected if not used. |
| **PCISTP#** / GPO6 | **AD6** | **O** | **PCI Clock Stop** (RxE4[1] = 0). Signals the system clock generator to disable the PCI clock outputs. Not connected if not used. |
| **SUSA#** / GPO1 | **AA2** | **O** | **Suspend Plane A Control** (Rx94[2]=0). Asserted during power management POS, STR, and STD suspend states. Used to control the primary power plane. (10K PU to VSUS33 if not used) |
| **SUSB#** / GPO2 | **AD3** | **O** | **Suspend Plane B Control** (Rx94[3]=0). Asserted during power management STR and STD suspend states. Used to control the secondary power plane. (10K PU to VSUS33 if not used) |
| **SUSC#** | **AF2** | **O** | **Suspend Plane C Control.** Asserted during power management STD suspend state. Used to control the tertiary power plane. Also connected to ATX power-on circuitry. (10K PU to VSUS33 if not used) |

### Power Management and Event Detection (Continued)

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| **SUSST1#** / GPO3 | **Y3** | **O** | **Suspend Status 1** (Rx94[4] = 0). Typically connected to the North Bridge to provide information on host clock status. Asserted when the system may stop the host clock, such as Stop Clock or during POS, STR, or STD suspend states. Connect 10K PU to VSUS33. |
| **SUSCLK** | **AB3** | **O** | **Suspend Clock.** 32.768 KHz output clock for use by the North Bridge (e.g., KT400A, CLE266, or P4X400) for DRAM refresh purposes. Stopped during Suspend-to-Disk and Soft-Off modes. Connect 10K PU to VSUS33. |
| **CPUMISS** / GPI17 | **Y1** | **I** | **CPU Missing.** Used to detect the physical presence of the CPU chip in its socket. High indicates no CPU present. Connect to the CPUMISS pin of the CPU socket. The state of this pin may be read in the SMBus 2 registers. This pin may be used as CPUMISS and GPI17 at the same time. |
| **AOLGPI** / GPI18/ THRM# | **Y4** | **I** | **Alert On LAN.** The state of this pin may be read in the SMBus 2 registers. This pinmay be used as AOLGPI, GPI18 and THRM# all at the same time. |

### Strap Pins for VT8235 Version CE Configuration

| Signal Name | Pin # | Function | Description | Note |
|---|---|---|---|---|
| Strap_AUTO | **AE10** | **Auto Reboot** | L: Enable Auto Reboot **H: Disable Auto Reboot (Default)** | |
| SPKR | **AF8** | **CPU Frequency Strapping** | L: Enable CPU Frequency Strapping H: Disable CPU Frequency Strapping (Default) | |
| KBCS# | **AF10** | **Internal Keyboard** Controller | L: Disable internal KBC H: Enable internal KBC (Default) | |
| SDCS1# | **AF25** | Eliminate External LAN EEPROM | L: Enable. Use external EEPROM (Default) H: Disable. Do not use external EEPROM | |

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## Power and Ground

| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| VSUS33 | AA4, AB4-6 | P | **Suspend Power.** 3.3V ±5%. Always available unless the mechanical switch of the power supply is turned off. If the ihsoft-offlÉD state is not implemented, then this pin can be connected to VCC33. Signals powered by or referenced to this plane are: PWRGD, RSMRST#, PWRBTN#, SMBCK1/2, SMBDT1/2, GPO0, SUSA# / GPO1, SUSB# / GPO2, SUSC#, SUSST1# / GPO3, SUSCLK / GPO4, GPI1, GPI2 / EXTSMI#, GPI3 / RING#, GPI4 / LID, GPI5 / BATLOW#, GPI6 / PME#, SMBALRT# |
| VSUS25 | T4, U4 | P | **Suspend Power.** 2.5V ±5%. |
| VSUSUSB | C24 | P | **USB Suspend Power.** 2.5V ±5%. |
| VBAT | AF4 | P | **RTC Battery.** Battery input for internal RTC (RTCX1, RTCX2) |
| VLVREF | H22 | P | **V-Link Voltage Reference.** 0.9V ±5% for 4x transfers and 0.625V ±5% for 8x transfers. |
| VLCOMP | J22 | AI | **V-Link Compensation.** |
| VCCVK | (see pin list) | P | **V-Link Compensation Circuit Voltage.** 2.5V ±5% |
| MIIVCC | D9, E9-11 | P | **LAN MII Power.** 3.3V ±5%.Power for LAN Media Independent Interface (interface to external PHY). Connect to VCC33 through a ferrite bead. |
| MIIVCC25 | D12. E12 | P | **LAN MII Suspend Power.** 2.5V ±5%. |
| LANVCC | E7 | P | **LAN Power.** 2.5V ±5%. Power for LAN. Connect to VCC through a ferrite bead. |
| LANGND | E6 | P | **LAN Ground.** Connect to GND through a ferrite bead. |
| USBVCC | (see pin list) | P | **USB 2.0 Differential Output Power.** 3.3V ±5%. Power for USB differential outputs (USBP0+, P0Œ, P1+, P1Œ, P2+, P2Œ, P3+, P3Œ, P4+, P4Œ, P5+, P5Œ). Connect to VSUS33 through a ferrite bead. |
| USBGND | (see pin list) | P | **USB 2.0 Differential Output Ground.** Connect to GND through a ferrite bead. |
| VCCUPLL | A23, B23 | P | **USB 2.0 PLL Analog Voltage.** 2.5V ±5%. Connect to VCC through a ferrite bead. |
| GNDUPLL | C23, D23 | P | **USB 2.0 PLL Analog Ground.** Connect to GND through a ferrite bead. |
| PLLVCC | T22 | P | **PLL Analog Power.** 2.5V ±5%. Connect to VCC through a ferrite bead. |
| PLLGND | U22 | P | **PLL Analog Ground.** Connect to GND through a ferrite bead. |

## Power and Ground ( Continued )

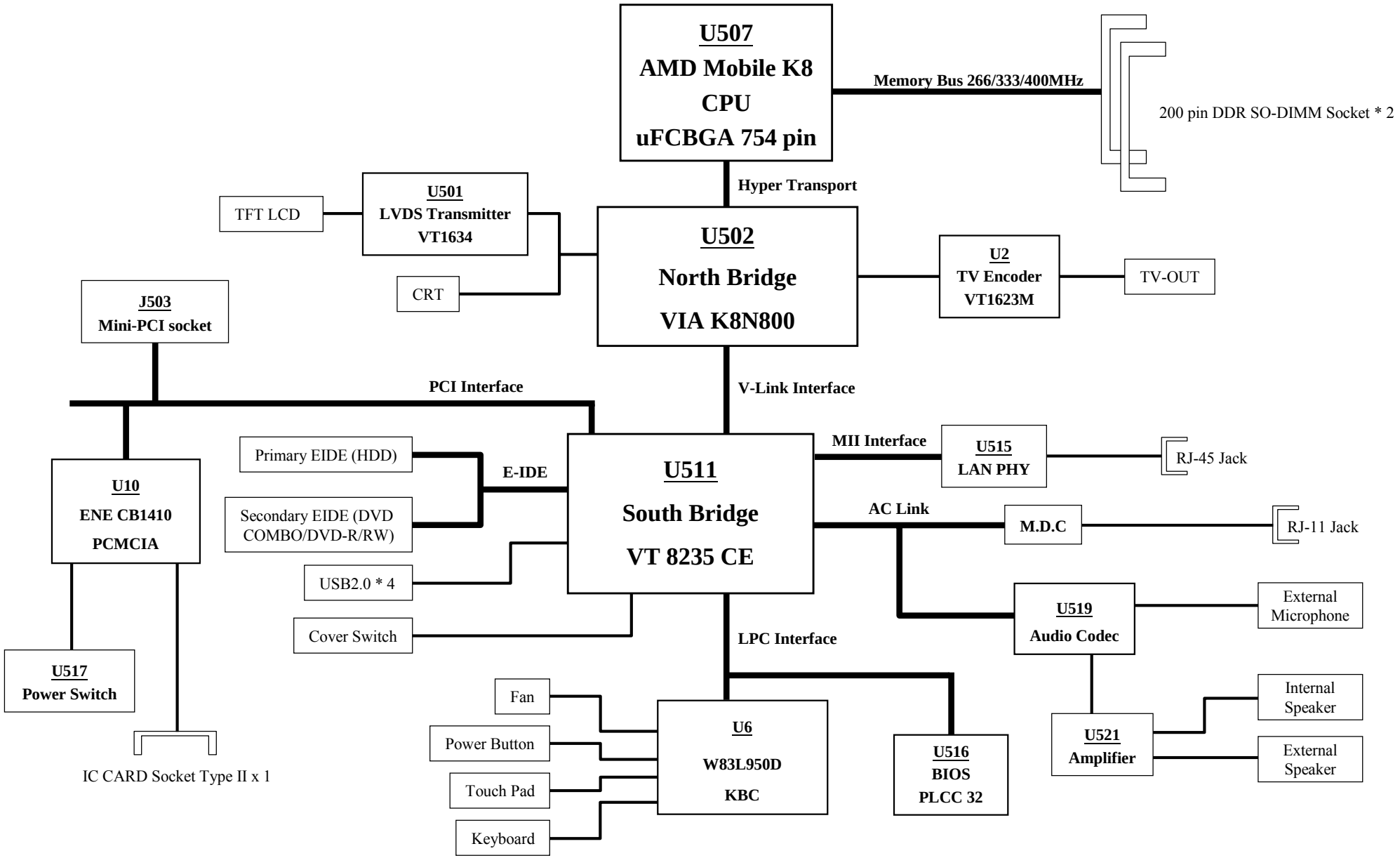
| Signal Name | Pin # | I/O | Signal Description |
|---|---|---|---|
| VCC33 | (see pin list) | P | I/O Power. **3.3V ±5%** |
| VCC | (see pin list) | P | Core Power. **2.5V ±5%. This supply is turned on only when the mechanical switch on the power supply is turned on and the PWRON signal is conditioned high.** |
| GND | (see pin list) | P | **Ground.** Connect to primary motherboard ground plane. |

## Strap Pins for North Bridge Configuration

| Signal Name | Pin # | Function | Description | Note |
|---|---|---|---|---|
| SDCS3# | AF26 | NB Configuration | SDCS3# signal state is reflected on signal pinVD[7] during power up for North Bridgeconfiguration. | **Check the NorthBridge DS fordetails** |
| SDA2 | AE24 | NB Configuration | SDA2 signal state is reflected on signal pinVD[6] during power up for North Bridgeconfiguration. | **Check the NorthBridge DS fordetails** |
| SDA1 | AC22 | NB Configuration | SDA1 signal state is reflected on signal pinVD[5] during power up for North Bridgeconfiguration. | **Check the NorthBridge DS fordetails** |
| SDA0 | AF24 | NB Configuration | SDA0 signal states is reflected on signal pinsVD[4] during power up for North Bridgeconfiguration. | **Check the NorthBridge DS fordetails** |
| Strap_VD3 | AC6 | NB Configuration | Strap_VD3 signal state is reflected on signal pinVD[3] during power up for North Bridgeconfiguration. | **Check the NorthBridge DS fordetails** |
| Strap_VD2 | AD5 | NB Configuration | Strap_VD2 signal state is reflected on signal pinVD[2] during power up for North Bridgeconfiguration. | **Check the NorthBridge DS fordetails** |
| Strap_VD1 | AE5 | NB Configuration | Strap_VD1 signal state is reflected on signal pin, VD[1] during power up for North Bridge configuration. | **Check the North Bridge DS for details** |
| Strap_VD0 | AF5 | NB Configuration | Strap_VD0 signal state is reflected on signalpin, VD[0] during power up for North Bridgeconfiguration. | **Check the NorthBridge DS fordetails** |

**Note:** Internal Pullups are present on pins KBCK, KBDT, MSCK, MSDT, SERIRQ, LAD[3:0]
Internal Pulldowns are present on all LAN pins

# 6. System Block Diagram



# 7. Maintenance Diagnostics

## 7.1 Introduction

Each time the computer is turned on, the system bios runs a series of internal checks on the hardware. This power-on self test (post) allows the computer to detect problems as early as the power-on stage. Error messages of post can alert you to the problems of your computer.

If an error is detected during these tests, you will see an error message displayed on the screen. If the error occurs before the display is initialized,then the screen cannot display the error message. Error codes or system beeps are used to identify a post error that occurs when the screen is not available.

The value for the diagnostic port (378H) is written at the beginning of the test. Therefore, if the test failed, the user can determine where the problem occurred by reading the last value written to port 378H by the 378H port debug board plug at Mini PCI Slot.

## 7.2 Error Codes (1)

**Following is a list of error codes in sequent display on the PIO debug board.**

| Code | POST Routine Description |
|---|---|
| 10h | Signals that Reset occurred |
| 11h | Turn off FAST A20 for POST |
| 12h | Signal power on reset |
| 13h | Initialize the chipset |
| 14h | Search for ISA Bus VGA adapter |
| 15h | Reset counter / Timer 1 |
| 16h | User register config through CMOS |
| 17h | Size memory |
| 18h | Dispatch to RAM test |
| 19h | Check sum the ROM |
| 1Ah | Reset PIC's |
| 1Bh | Initialize video adapter |
| 1Ch | Initialize video |
| 1Dh | Initialize color adapter |
| 1Eh | Initialize monochrome adapter |
| 1Fh | Test 8237A page registers |

| Code | POST Routine Description |
|---|---|
| 20h | Test keyboard |
| 21h | Test keyboard controller |
| 22h | Check if CMOS RAM valid |
| 23h | Test battery fail & CMOS X-SUM |
| 24h | Test DMA controller |
| 25h | Initialize 8237A controller |
| 26h | Initialize int vectors |
| 27h | RAM quick sizing |
| 28h | Protected mode entered safely |
| 29h | RAM test completed |
| 2Ah | Protected mode exit successful |
| 2Bh | Setup shadow |
| 2Ch | Going to initialize video |
| 2Dh | Search for monochrome adapter |
| 2Eh | Search for color adapter |
| 2Fh | Sign-on messages displayed |

## 7.2 Error Codes (2)

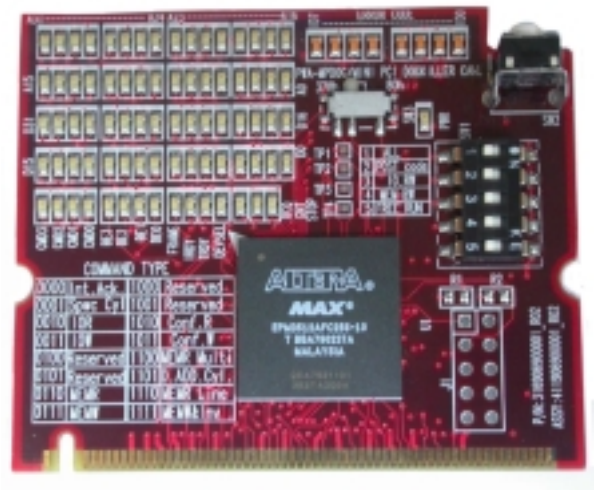
**Following is a list of error codes in sequent display on the PIO debug board.**

| Code | POST Routine Description |
|---|---|
| 30h | OEM initialization of keyboard controller |
| 31h | Test if keyboard Present |
| 32h | Test keyboard Interrupt |
| 33h | Test keyboard command byte |
| 34h | Test, blank and count all RAM |
| 35h | Protected mode entered safely(2) |
| 36h | RAM test complete |
| 37h | Protected mode exit successful |
| 38h | Update keyboard controller output port |
| 39h | Setup cache controller |
| 3Ah | Test if 18.2Hz periodic working |
| 3Bh | Test for RTC ticking |
| 3Ch | Initialize the hardware vectors |
| 3Dh | Search for and initialize the mouse |
| 3Eh | Update NUMLOCK status |
| 3Fh | OEM initialization of COM and LPT ports |

| Code | POST Routine Description |
|---|---|
| 40h | Configure the COMM and LPT ports |
| 41h | Initialize the floppies |
| 42h | Initialize the hard disk |
| 43h | Initialize option ROMs |
| 44h | OEM's initialization of power management |
| 45h | Update NUMLOCK status |
| 46h | Test for coprocessor installed |
| 47h | OEM functions before boot |
| 48h | Dispatch to operate system boot |
| 49h | Jump into bootstrap code |

## 7.3 Debug Tool

### 7.3.1 Diagnostic Tool  for Mini PCI Slot :




P/N:411906900001
Description: PWA-MPDOG;MINI PCI DOGKELLER CARD
Note: Order it from MIC/TSSC

# 8. Trouble Shooting

- 8.1 No Power (*1)
- 8.2 Battery Can not Be Charged
- 8.3 No Display (*2)
- 8.4 LCD No Display or Picture Abnormal
- 8.5 External Monitor No Display or Color Abnormal
- 8.6 TV Test Error
- 8.7 Memory Test Error
- 8.8 Keyboard (K/B) Touch-Pad (T/P) Test Error
- 8.9 Hard Drive Test Error
- 8.10 CD-ROM Driver Test Error
- 8.11 USB Port Test Error
- 8.12 PC Card Socket Test Error
- 8.13 Mini-PCI Socket Test Error
- 8.14 Audio Failure
- 8.15 LAN Test Error

# 8889 N/B Maintenance

## *1: No power definition

Base on ACPI Spec. We define the no power as while we press the power button, the system can't leave S5 status or none the PG signal send out from power supply.

Judge condition:

- Check whether there are any voltage feedback control to turn off the power.
- Check whether no CPU power will cause system can't leave S5 status.

If there are not any diagram match these condition, we should stop analyzing the schematic in power supply sending out the PG signal. If yes, we should add the effected analysis into no power chapter.

## *2: No display definition

Base on the digital IC three basic working conditions: working power, reset, Clock. We define the no display as while system leave S5 status but can't get into S0 status.

Judge condition:

- Check which power will cause no display.
- Check which reset signal will cause no display.
- Check which Clock signal will cause no display

Base on these three conditions to analyze the schematic and edit the no display chapter.

## Keyword:

- S5: *Soft Off*
- S0: *Working*

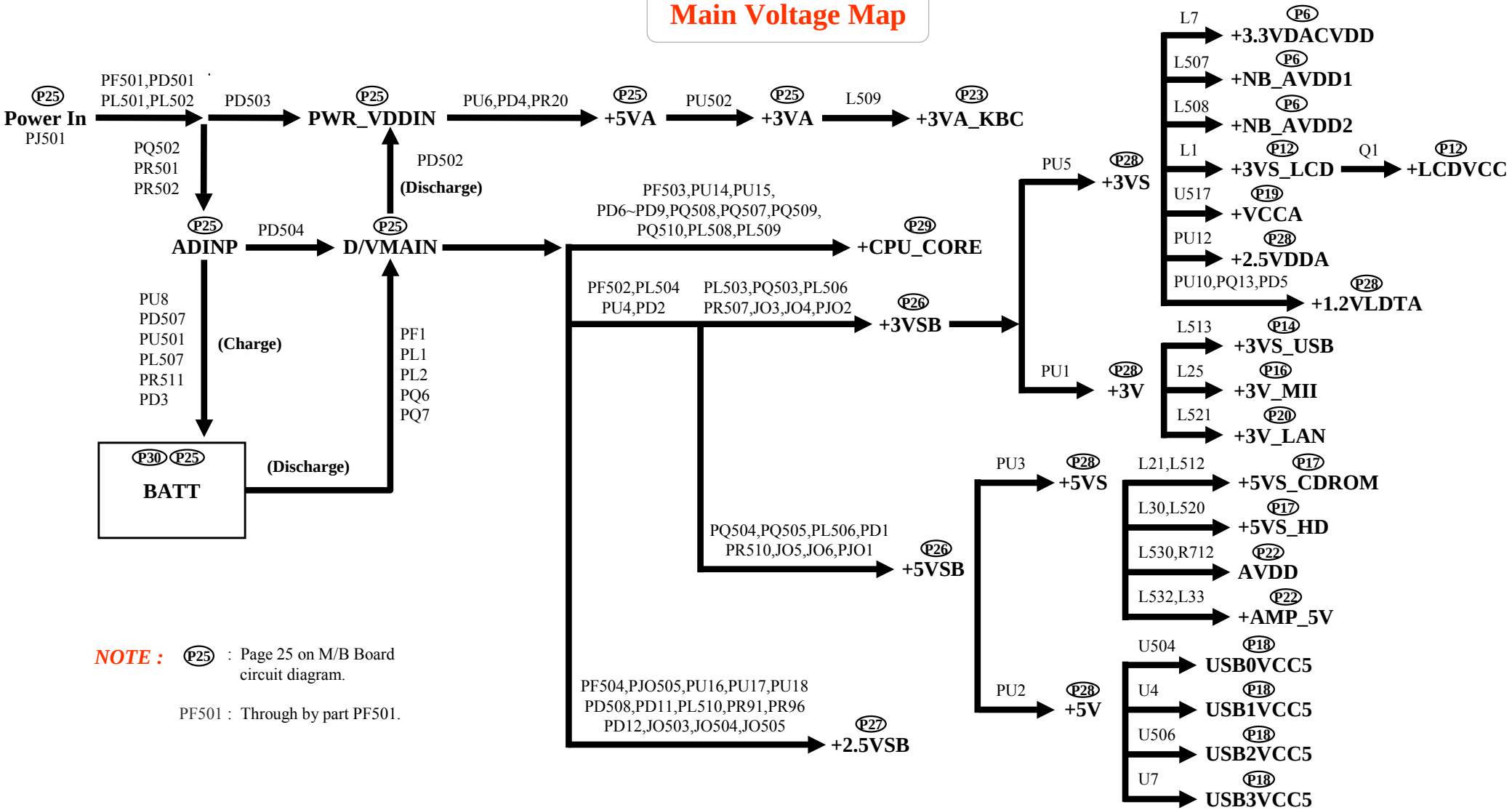
For detail please refer the ACPI specification

# 8889 N/B Maintenance

## 8.1 No Power (1)

**When power button is pressed ,nothing happens ,power indicator does not light up.**

**Main Voltage Map**




***NOTE :*** P25 : Page 25 on M/B Board circuit diagram.

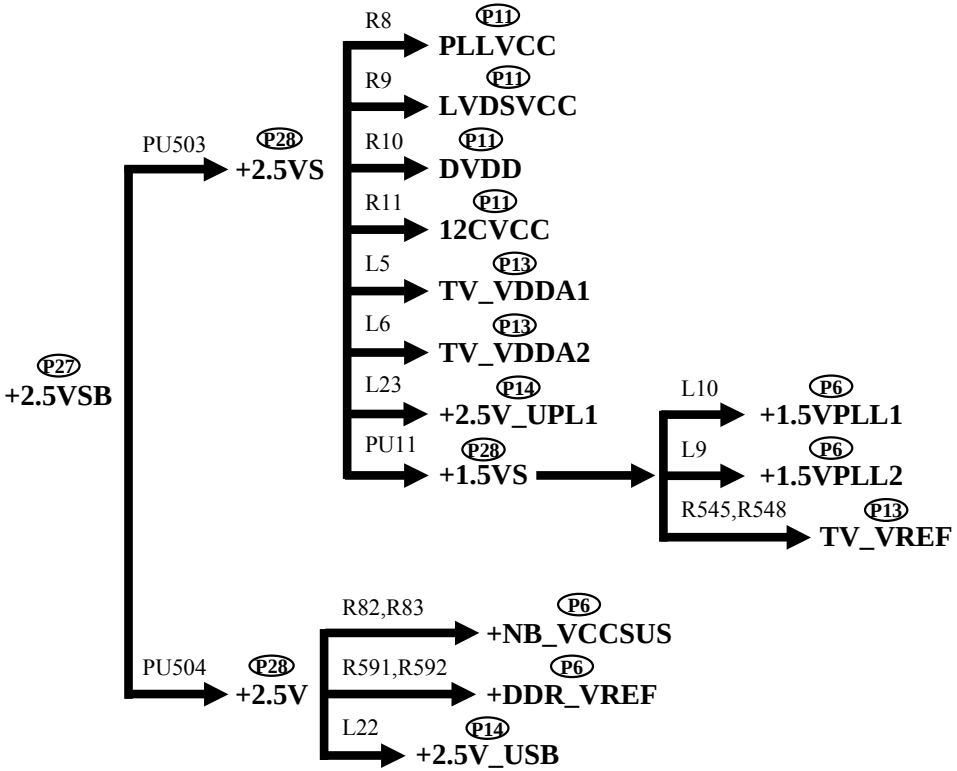
PF501 : Through by part PF501.

## 8.1 No Power (2)

**When power button is pressed ,nothing happens ,power indicator does not light up.**

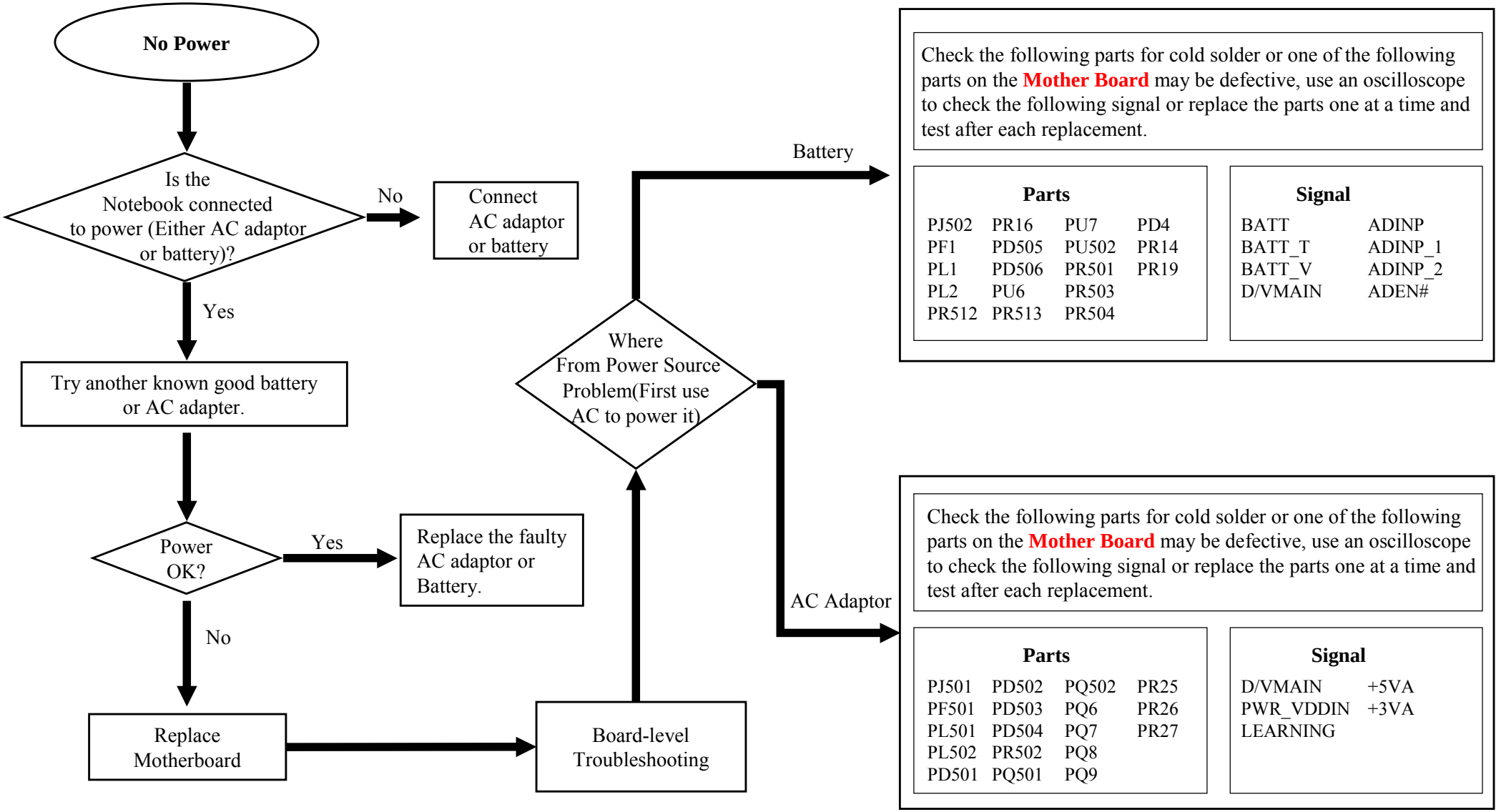
Main Voltage Map

Continue to the previous page



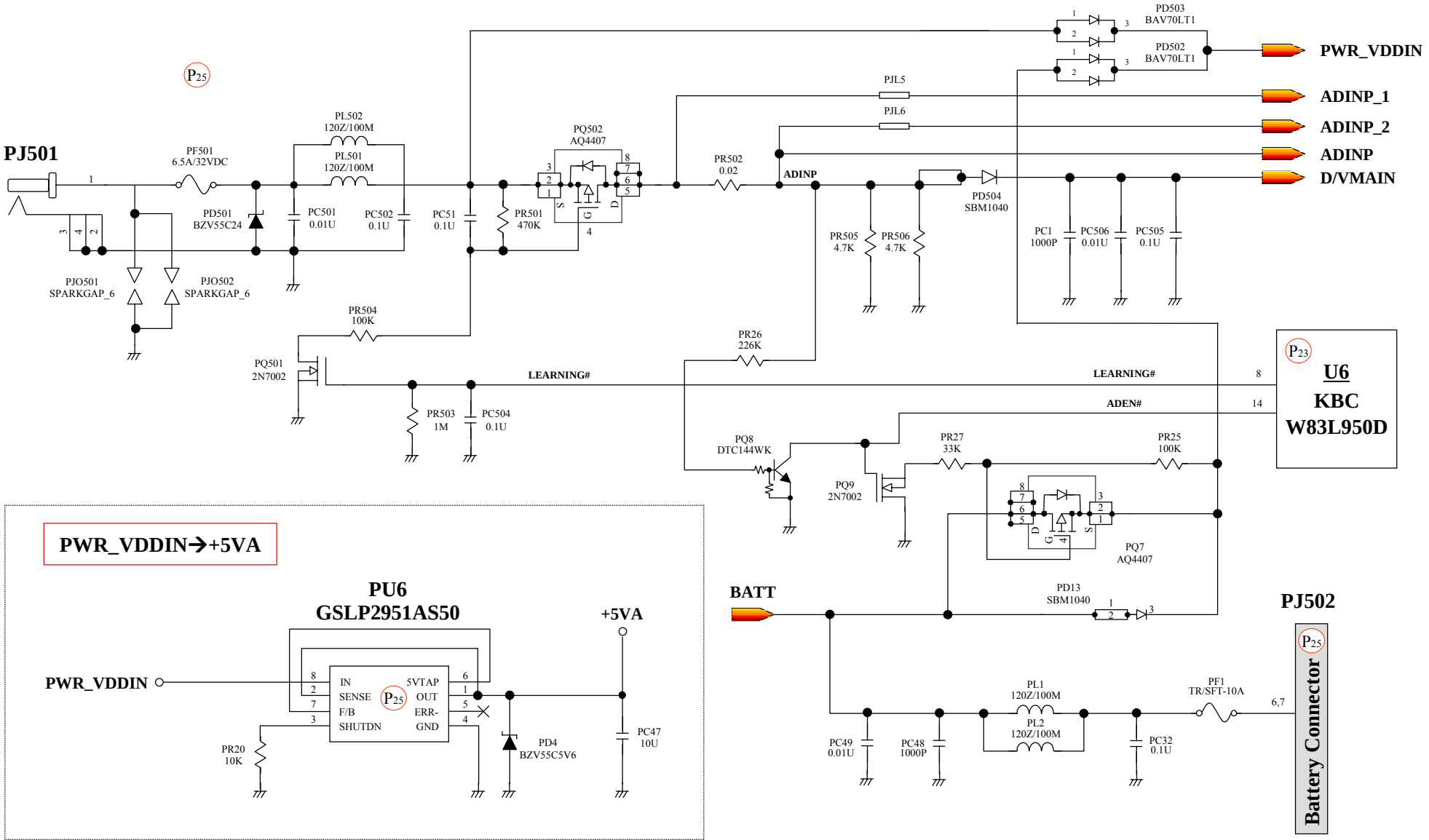
## 8.1 No Power (3)

**When power button is pressed ,nothing happens ,power indicator does not light up.**


No Power
Is the Notebook connected to power (Either AC adaptor or battery)?
No
Connect AC adaptor or battery
Yes
Try another known good battery or AC adapter.
Power OK?
Yes
Replace the faulty AC adaptor or Battery.
No
Replace Motherboard
Board-level Troubleshooting
Where From Power Source Problem(First use AC to power it)
Battery
AC Adaptor
Check the following parts for cold solder or one of the following parts on the Mother Board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.
Parts
PJ502 PR16 PU7 PD4
PF1 PD505 PU502 PR14
PL1 PD506 PR501 PR19
PL2 PU6 PR503
PR512 PR513 PR504
Signal
BATT ADINP
BATT_T ADINP_1
BATT_V ADINP_2
D/VMAIN ADEN#
Check the following parts for cold solder or one of the following parts on the Mother Board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.
Parts
PJ501 PD502 PQ502 PR25
PF501 PD503 PQ6 PR26
PL501 PD504 PQ7 PR27
PL502 PR502 PQ8
PD501 PQ501 PQ9
Signal
D/VMAIN +5VA
PWR_VDDIN +3VA
LEARNING

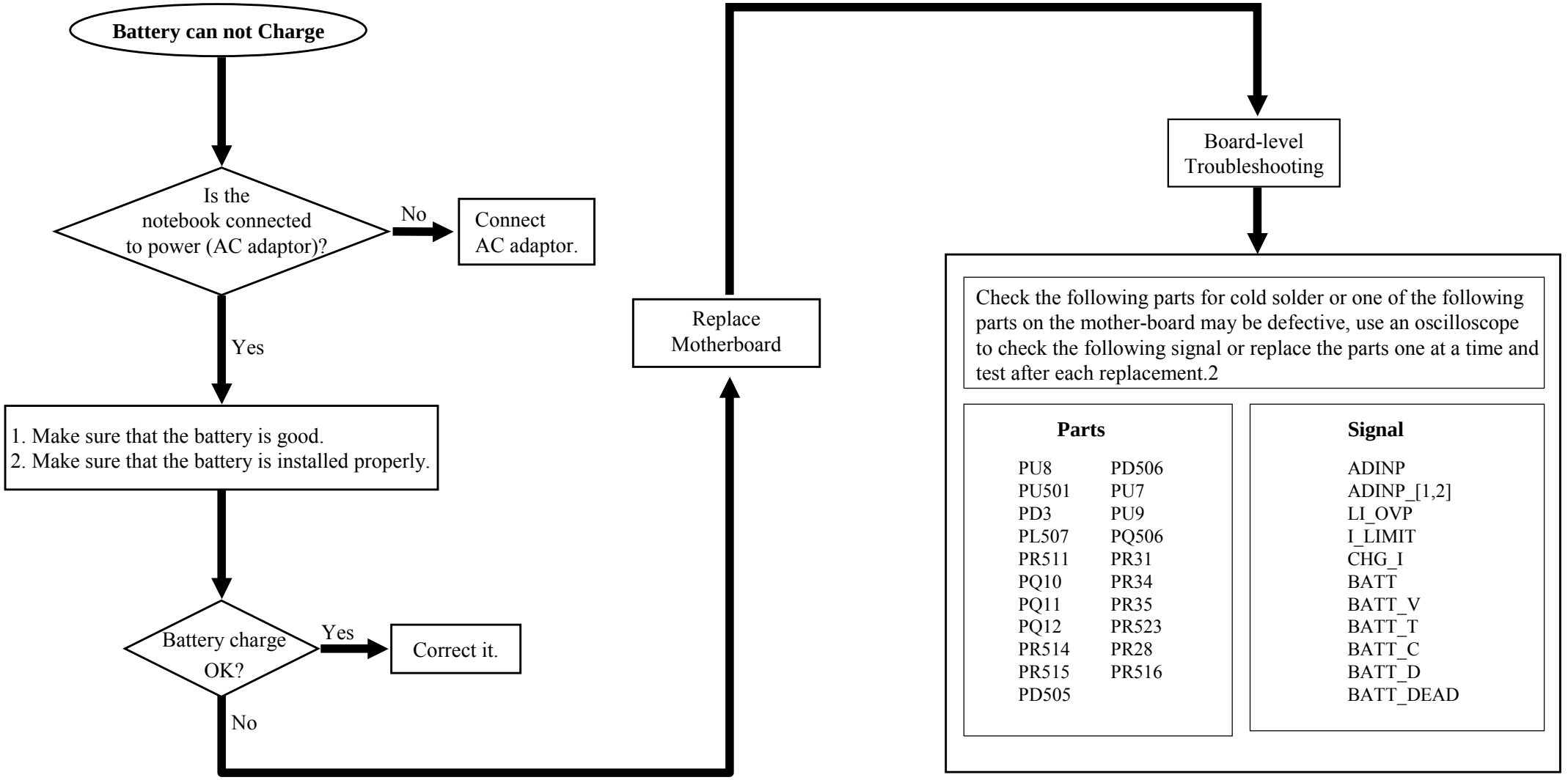
## 8.1 No Power (4)

**When power button is pressed ,nothing happens ,power indicator does not light up.**



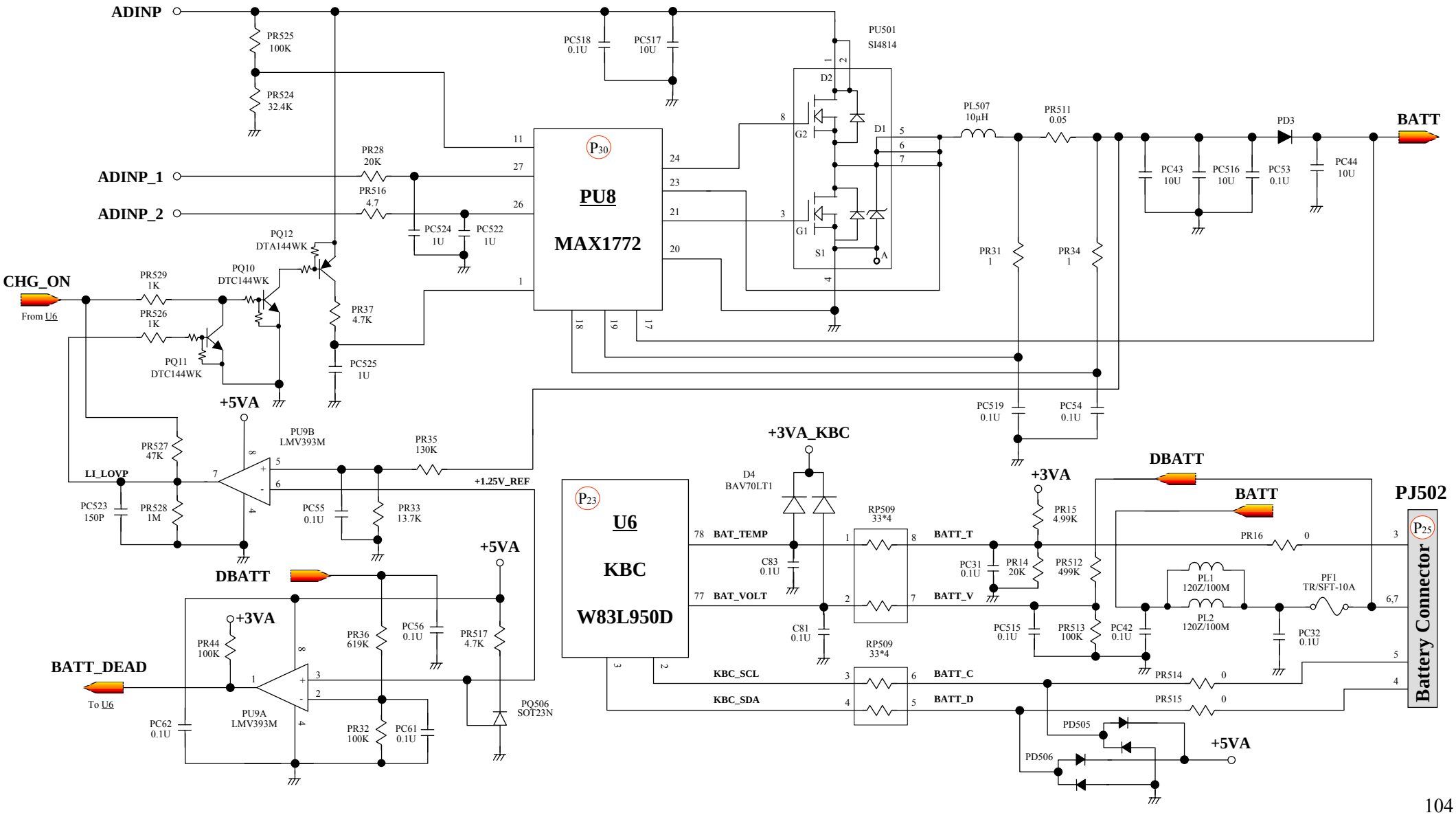
## 8.2 Battery Can not Be Charged (1)

**When the battery is installed but the battery status indicate LED display abnormal.**



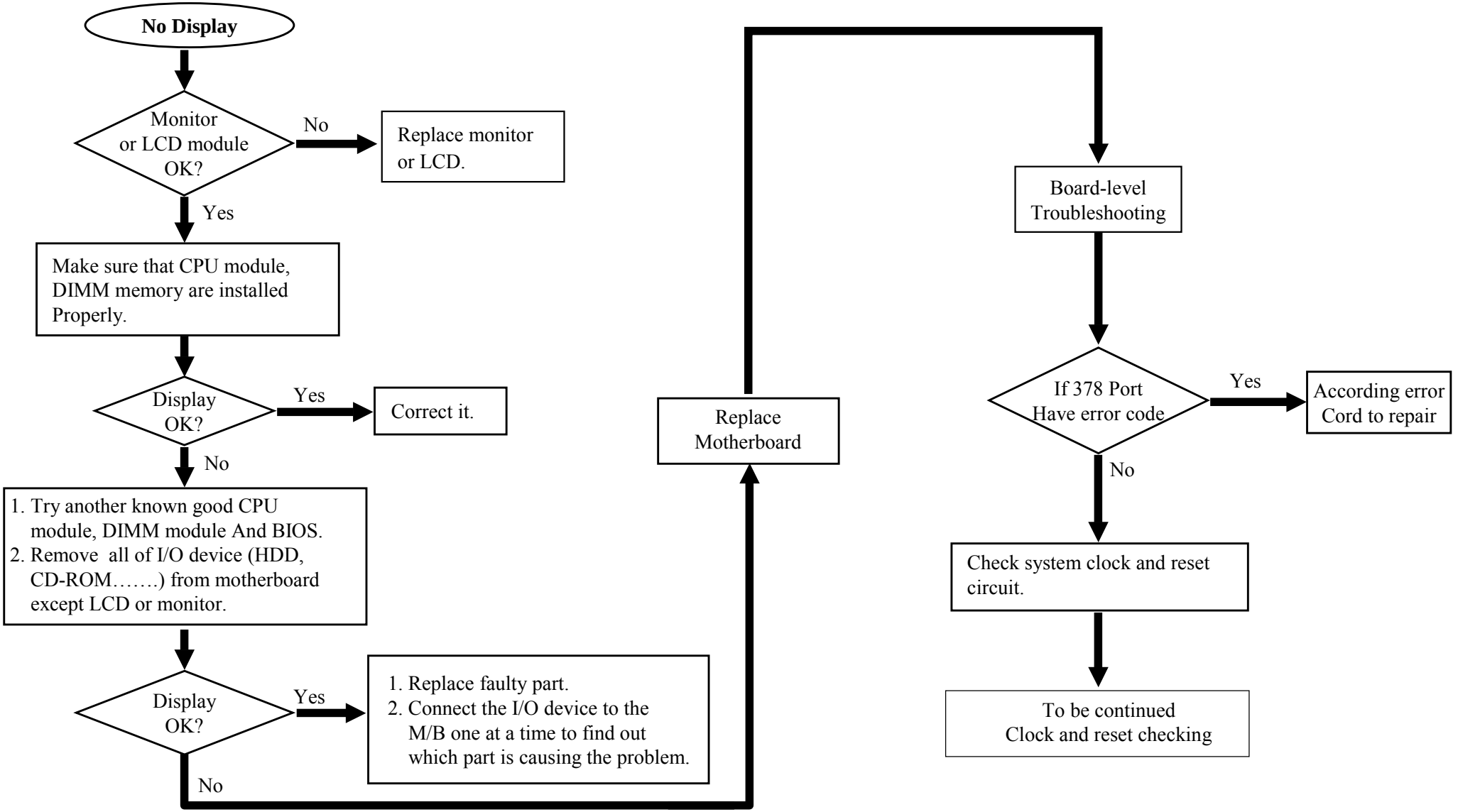
## 8.2 Battery Can not Be Charged (2)

**When the battery is installed but the battery status indicate LED display abnormal.**



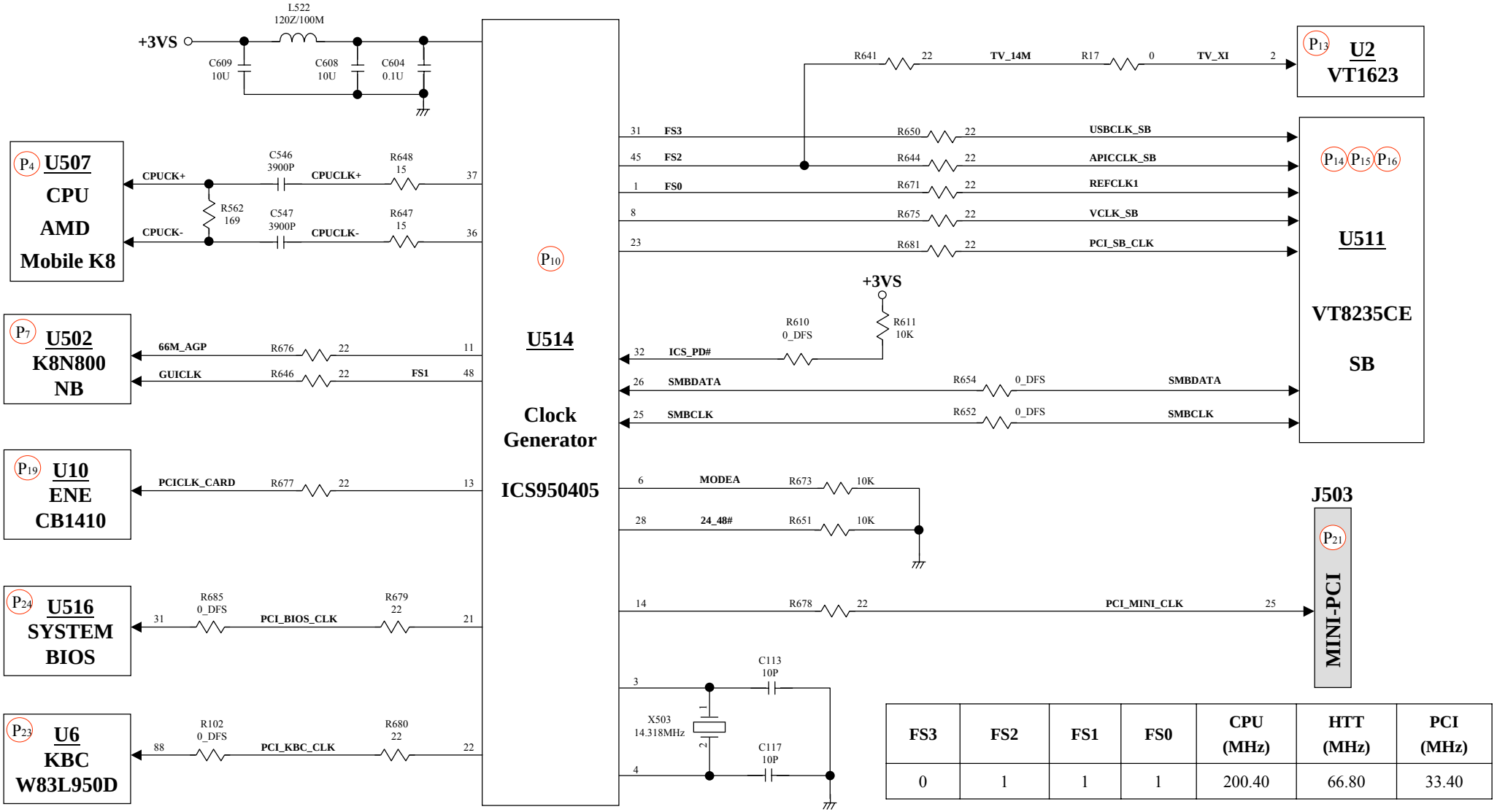
## 8.3 No Display (1)

**There is no display on both LCD and VGA monitor after power on although the LCD and monitor is known-good.**


No Display
Monitor or LCD module OK?
No
Replace monitor or LCD.
Yes
Make sure that CPU module, DIMM memory are installed Properly.
Display OK?
Yes
Correct it.
No
1. Try another known good CPU module, DIMM module And BIOS.
2. Remove all of I/O device (HDD, CD-ROM…….) from motherboard except LCD or monitor.
Display OK?
Yes
1. Replace faulty part.
2. Connect the I/O device to the M/B one at a time to find out which part is causing the problem.
No
Replace Motherboard
Board-level Troubleshooting
If 378 Port Have error code
Yes
According error Cord to repair
No
Check system clock and reset circuit.
To be continued
Clock and reset checking

## 8.3 No Display (2)

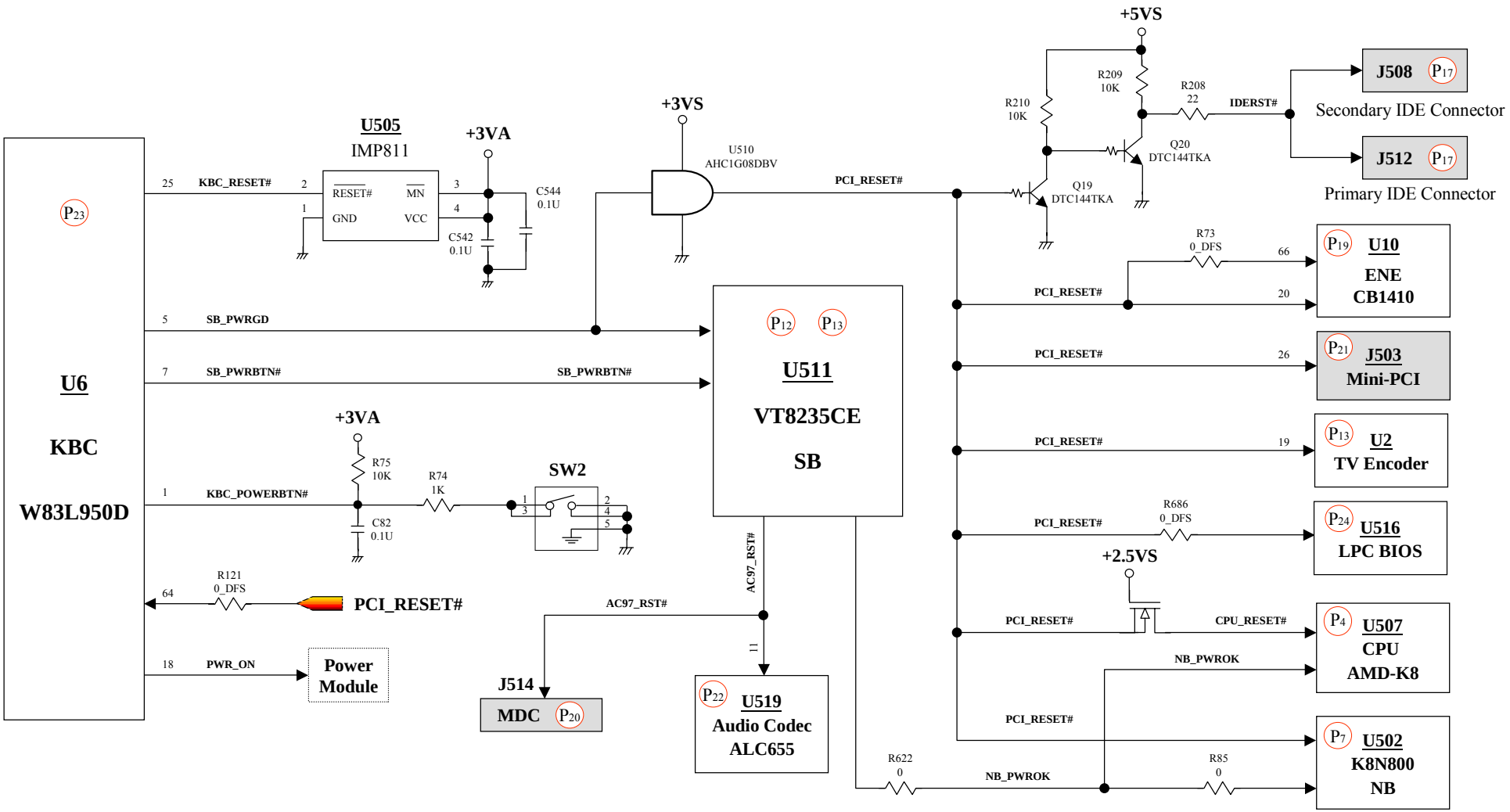
### System Clock Check




| FS3 | FS2 | FS1 | FS0 | CPU (MHz) | HTT (MHz) | PCI (MHz) |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 200.40 | 66.80 | 33.40 |

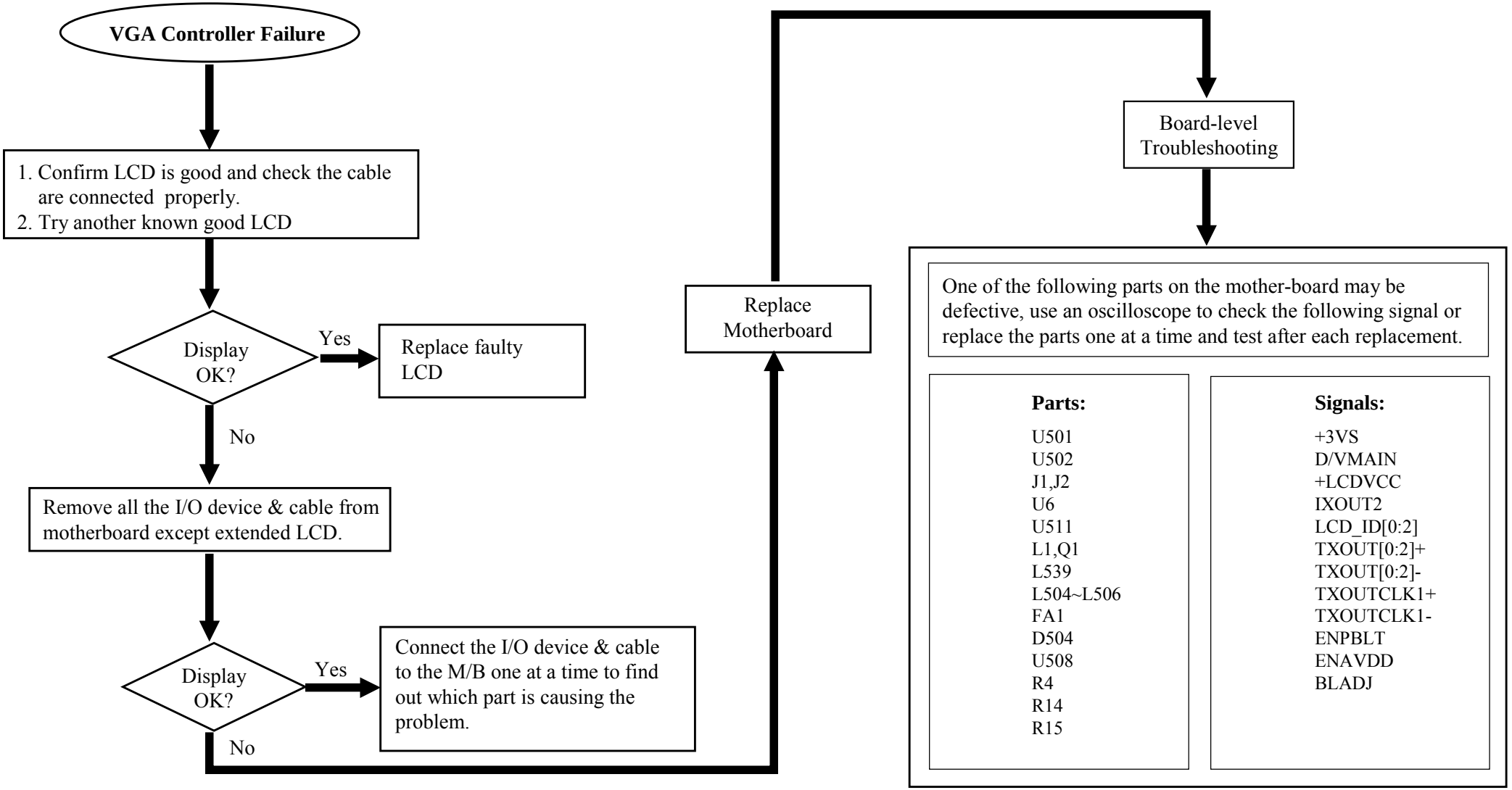
## 8.3 No Display (3)

### System Reset Check



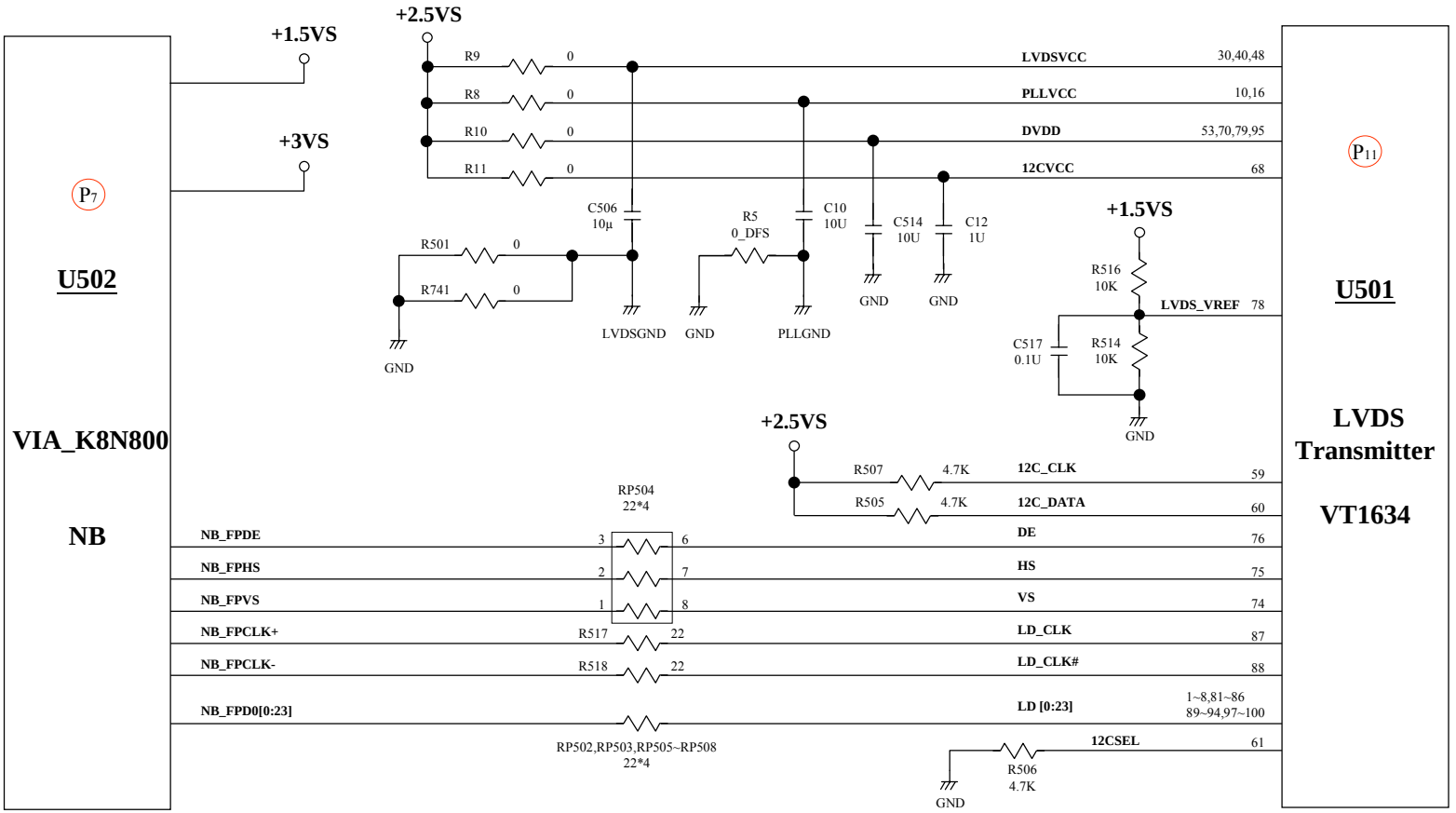
## 8.4 LCD No Display or Picture Abnormal (1)

**There is no display or picture abnormal on LCD or monitor.**



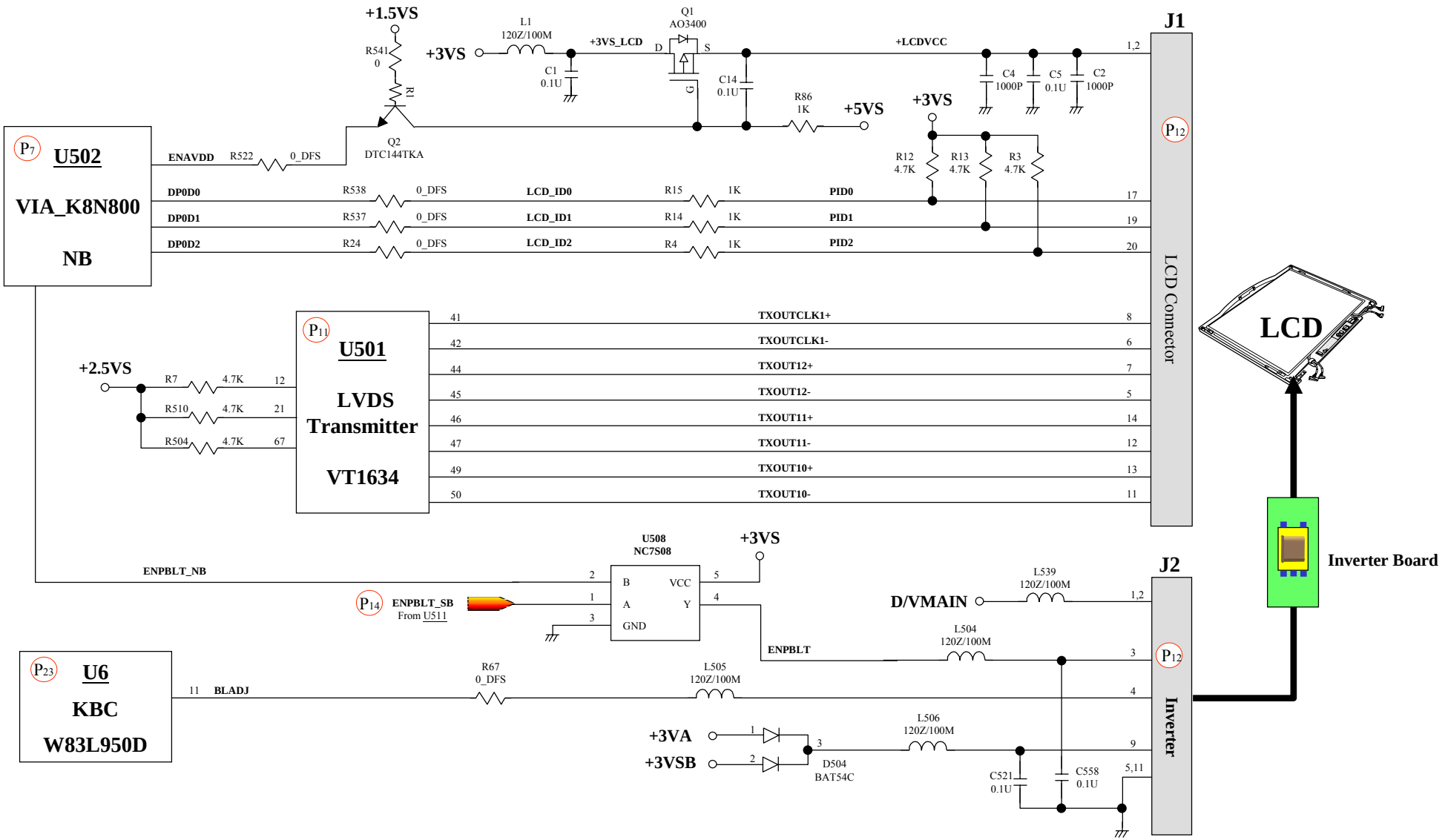
# 8.4 LCD No Display or Picture Abnormal (2)

**There is no display or picture abnormal on LCD or monitor.**



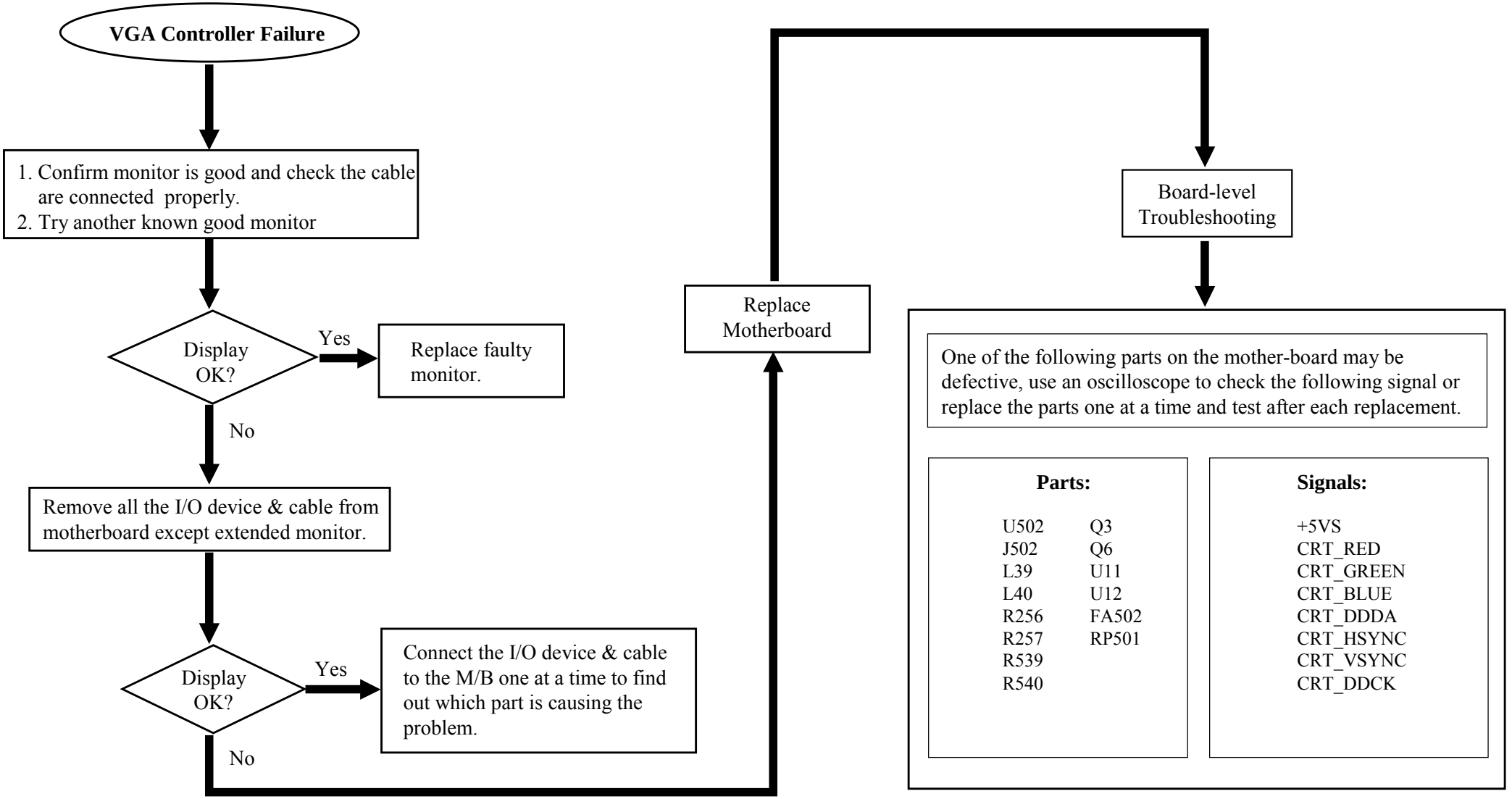
# 8.4 LCD No Display or Picture Abnormal (3)

**There is no display or picture abnormal on LCD or monitor.**



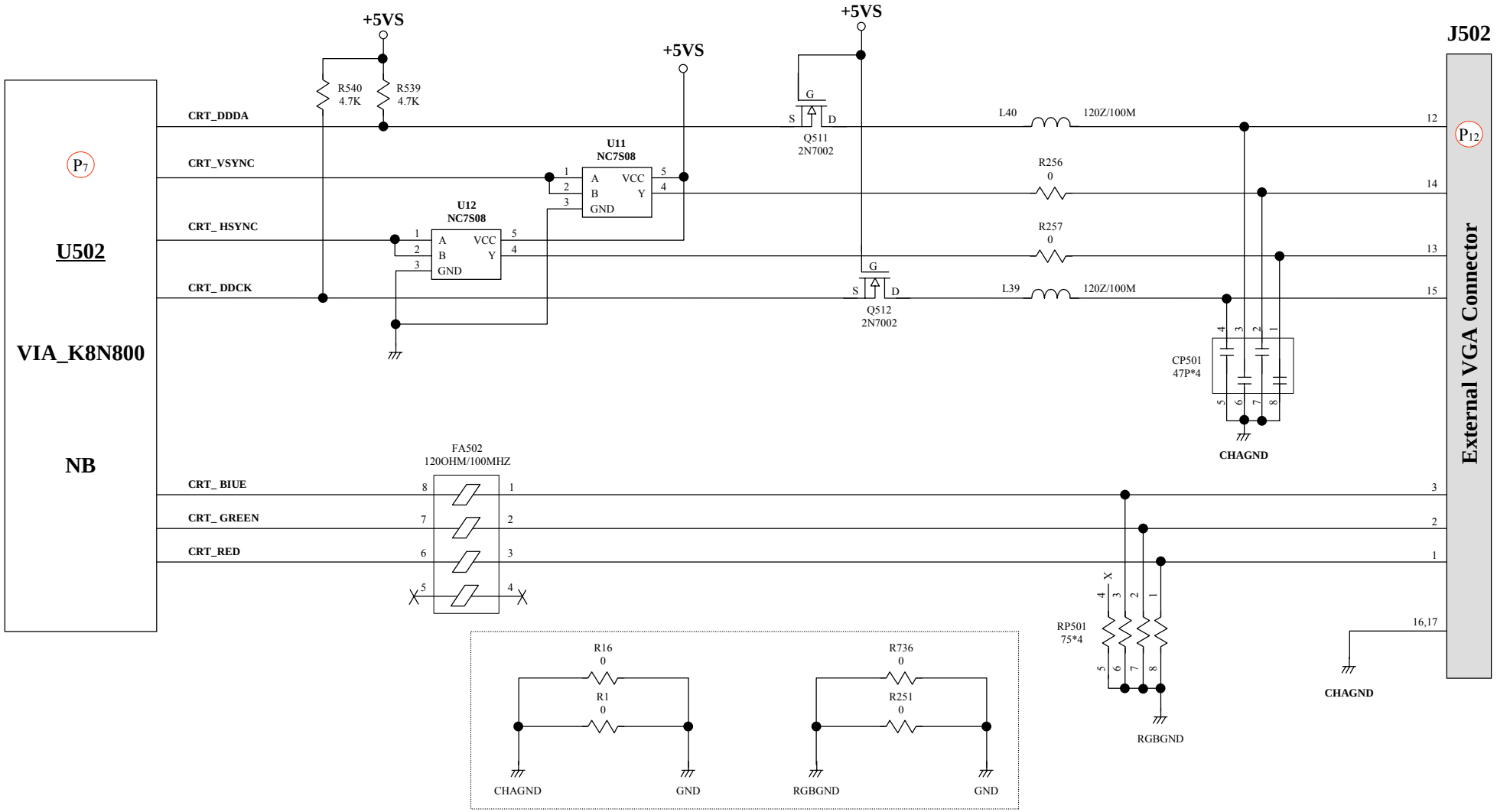
# 8.5 External Monitor No Display or Color Abnormal (1)

**There is no display or picture abnormal on monitor.**



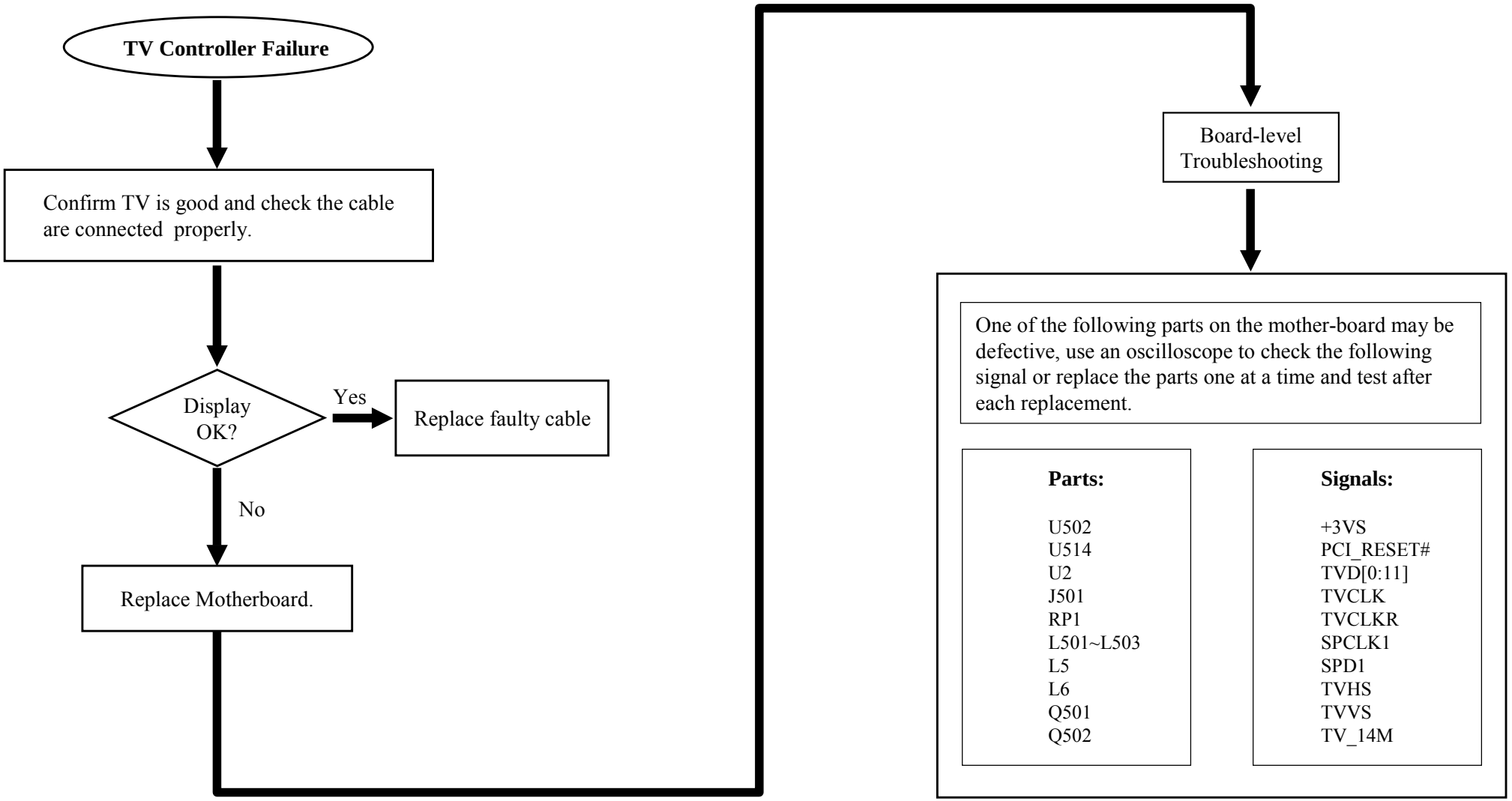
## 8.5 External Monitor No Display or Color Abnormal (2)

**There is no display or picture abnormal on monitor.**



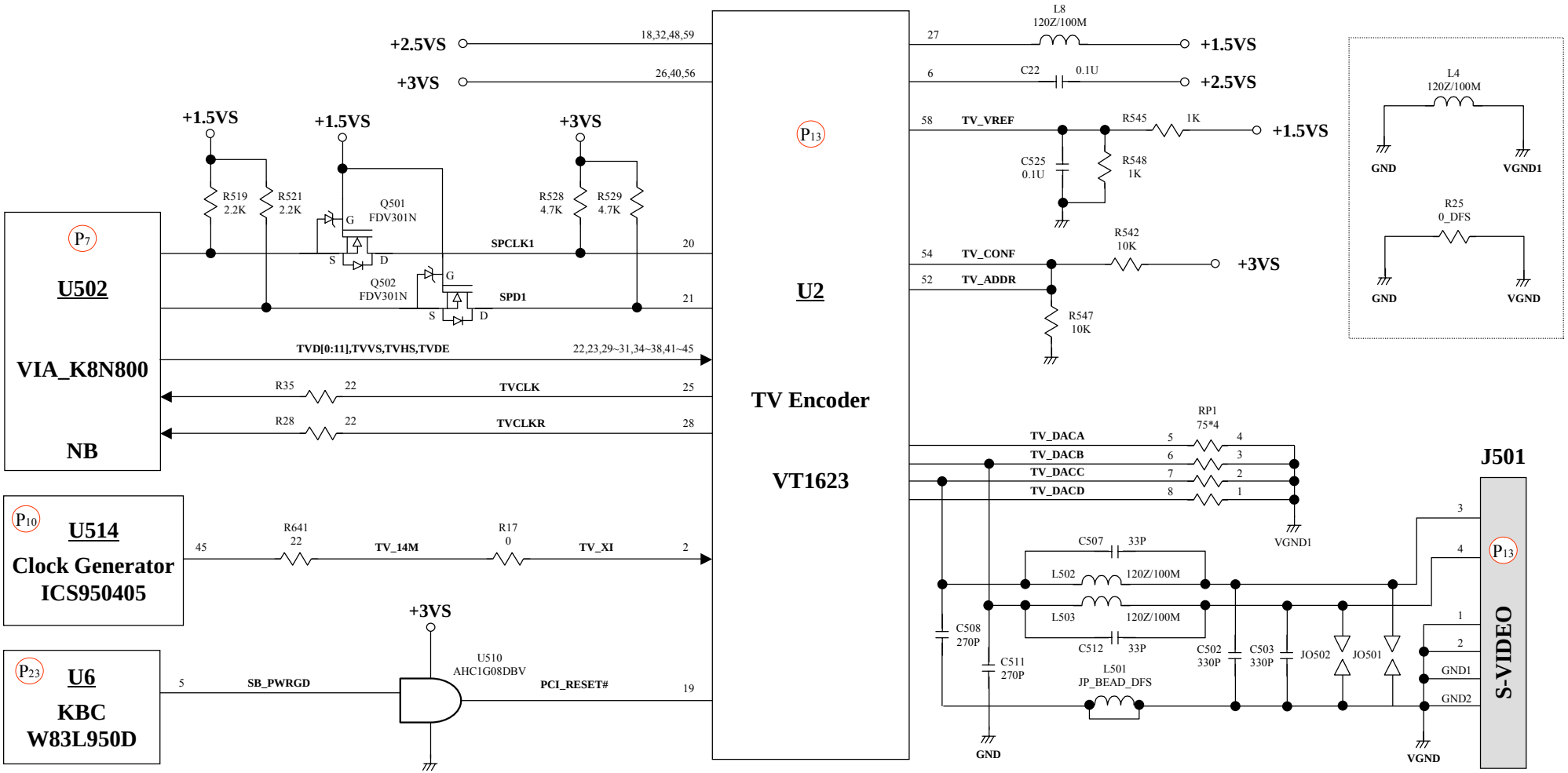
## 8.6 TV Test Error (1)

**There is no display or picture abnormal on TV.**



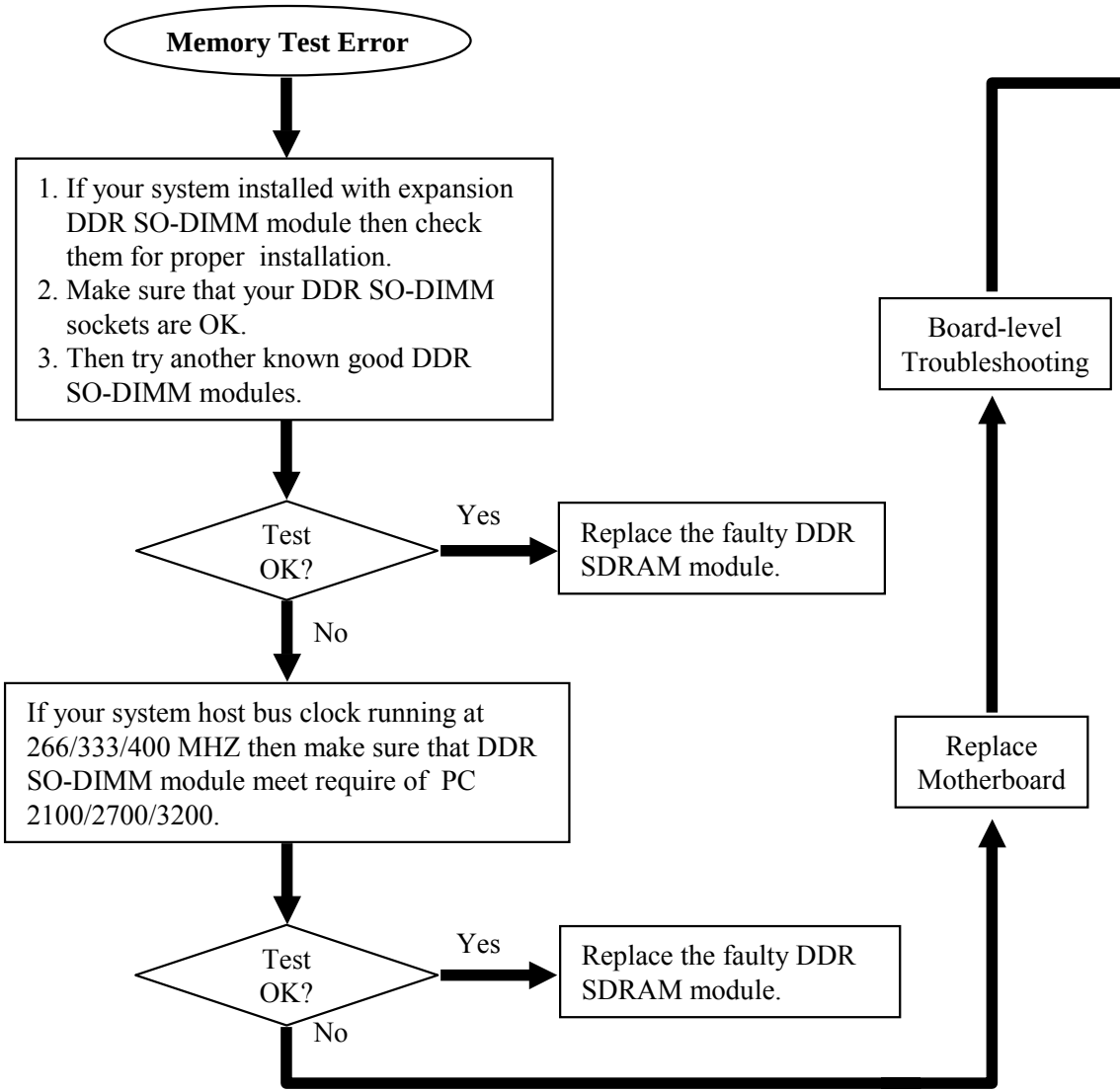
## 8.6 TV Test Error (2)

**There is no display or picture abnormal on TV.**



# 8.7 Memory Test Error (1)

**Extend DDRAM is failure or system hangs up.**


Memory Test Error
1. If your system installed with expansion DDR SO-DIMM module then check them for proper installation.
2. Make sure that your DDR SO-DIMM sockets are OK.
3. Then try another known good DDR SO-DIMM modules.
Test OK?
Yes
Replace the faulty DDR SDRAM module.
No
If your system host bus clock running at 266/333/400 MHZ then make sure that DDR SO-DIMM module meet require of PC 2100/2700/3200.
Test OK?
Yes
Replace the faulty DDR SDRAM module.
No
Replace Motherboard
Board-level Troubleshooting

One of the following components or signals on the motherboard may be defective ,Use an oscilloscope to check the signals or replace the parts one at A time and test after each replacement.

**Parts:**

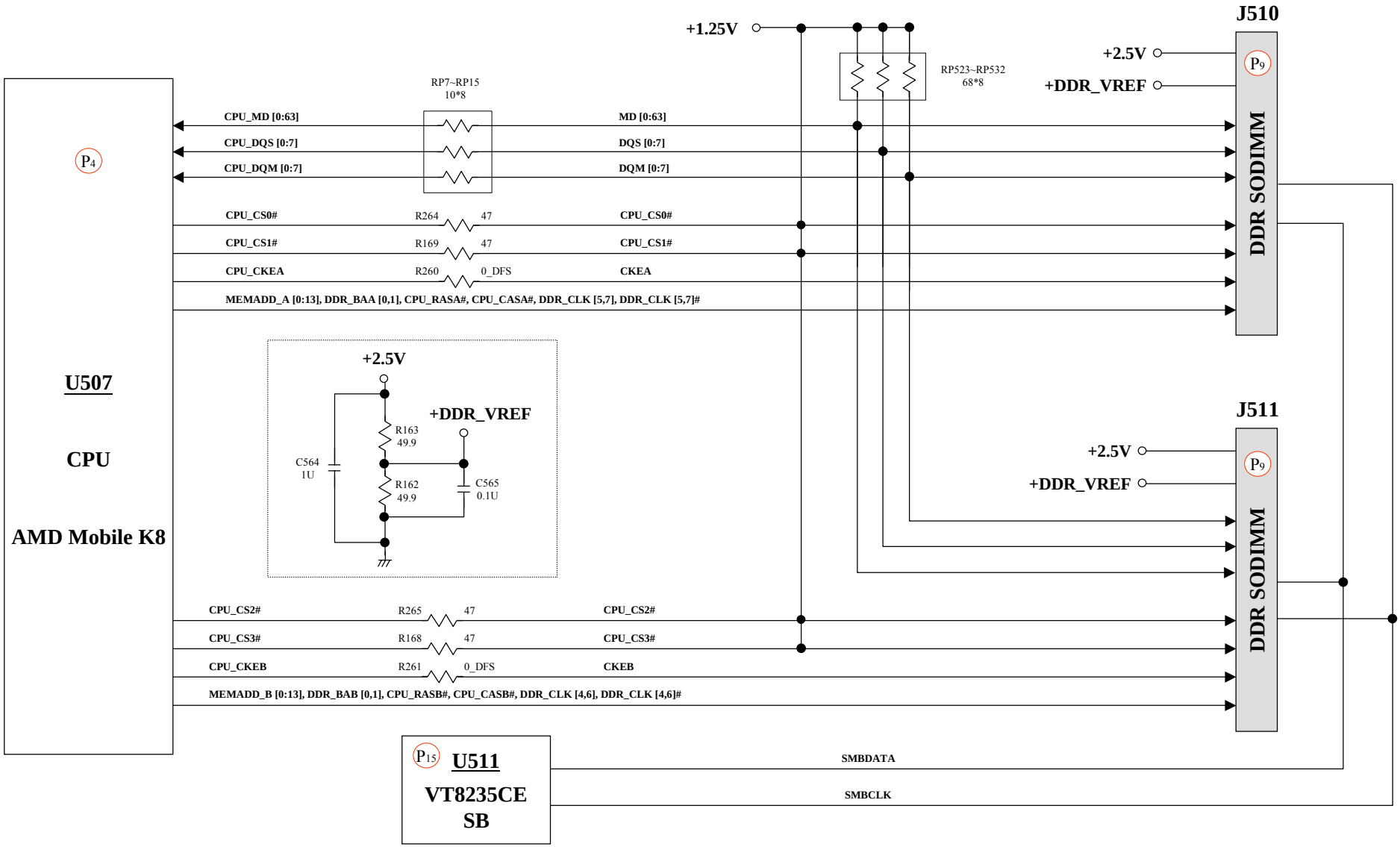
U507
U514
J510
J511
R587~R590
RP7~PR16
R168
R169
RP513~RP517
RP523~RP532
R652
R654

**Signals:**

+2.5V
+DDR_VREF
CKEA
CKEB
SMBDATA
SMBCLK
DDR_BAA [0,1]
DDR_BAB [0,1]
MEMADD_A[0:13]
MEMADD_B[0:13]
DDR_CLK [0,1,4,5,6,7]
DDR_CLK [0,1,4,5,6,7]#
DDR_WEA#
DDR_WEB#
CPU_CS[0:3]#
DDR_RASA#
DDR_RASB#
DDR_CASA#
DDR_CASB#

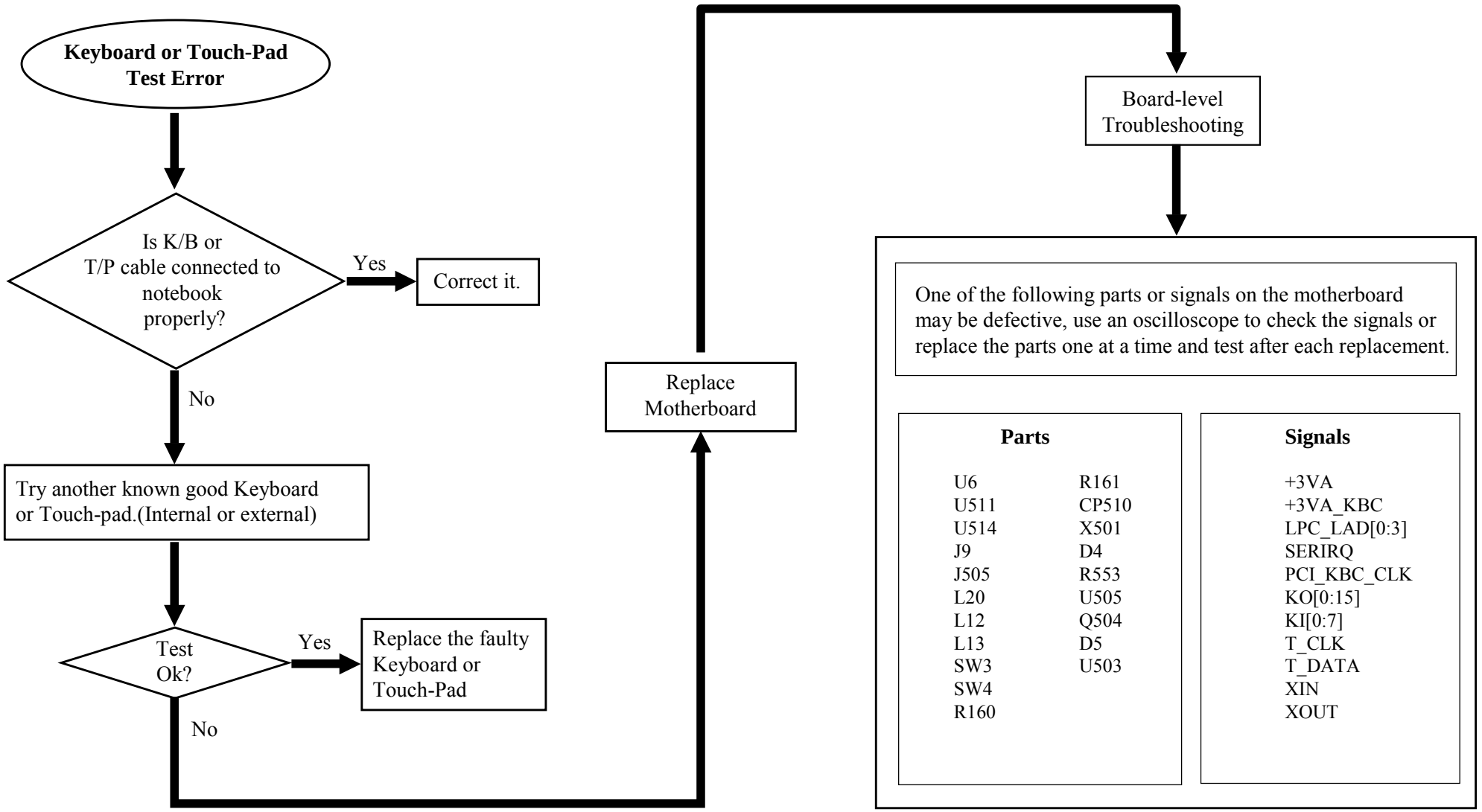
# 8.7 Memory Test Error (2)

**Extend DDRAM is failure or system hangs up.**



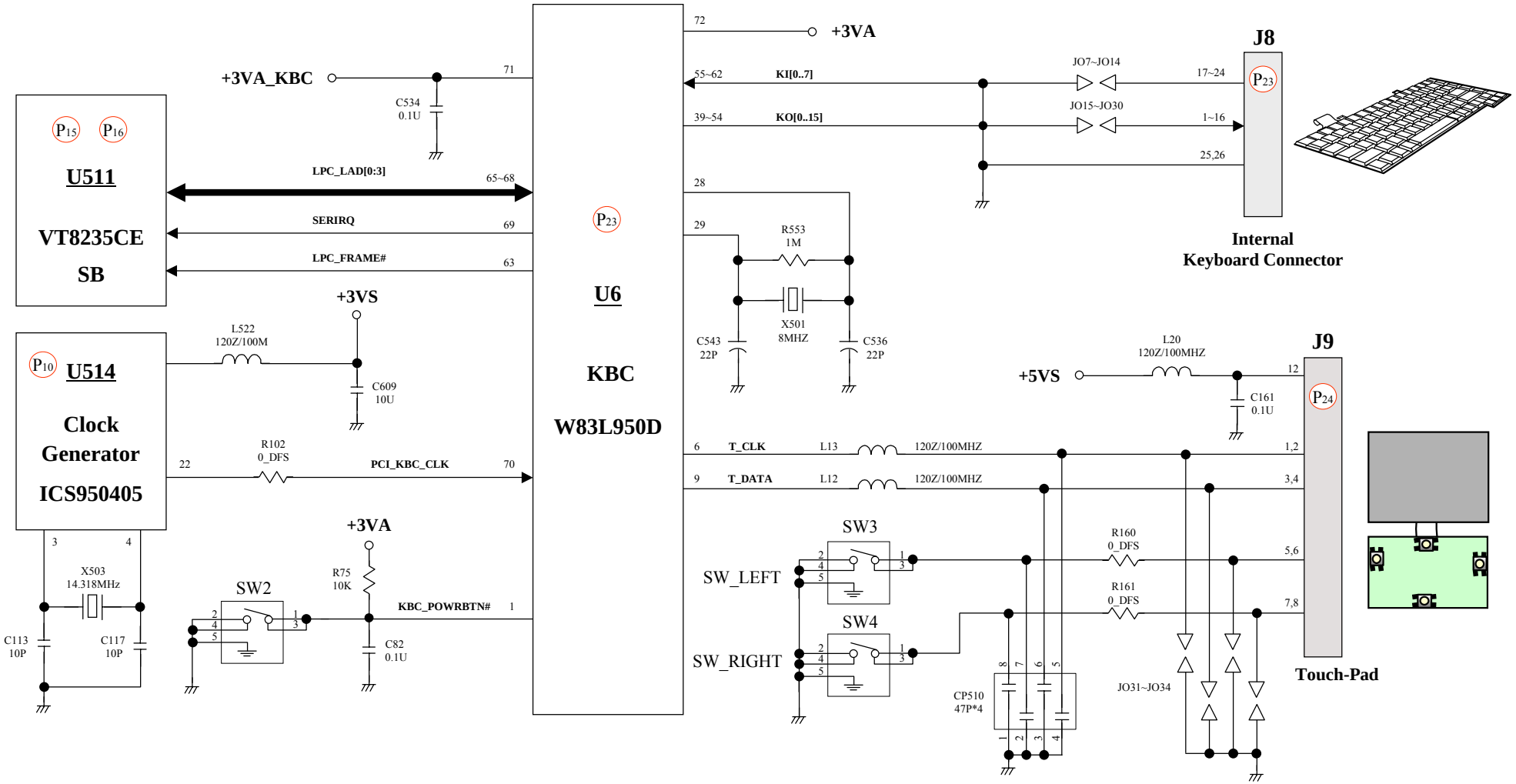
## 8.8 Keyboard (K/B) Touch-Pad (T/P) Test Error (1)

**Error message of keyboard or touch-pad failure is shown or any key does not work.**



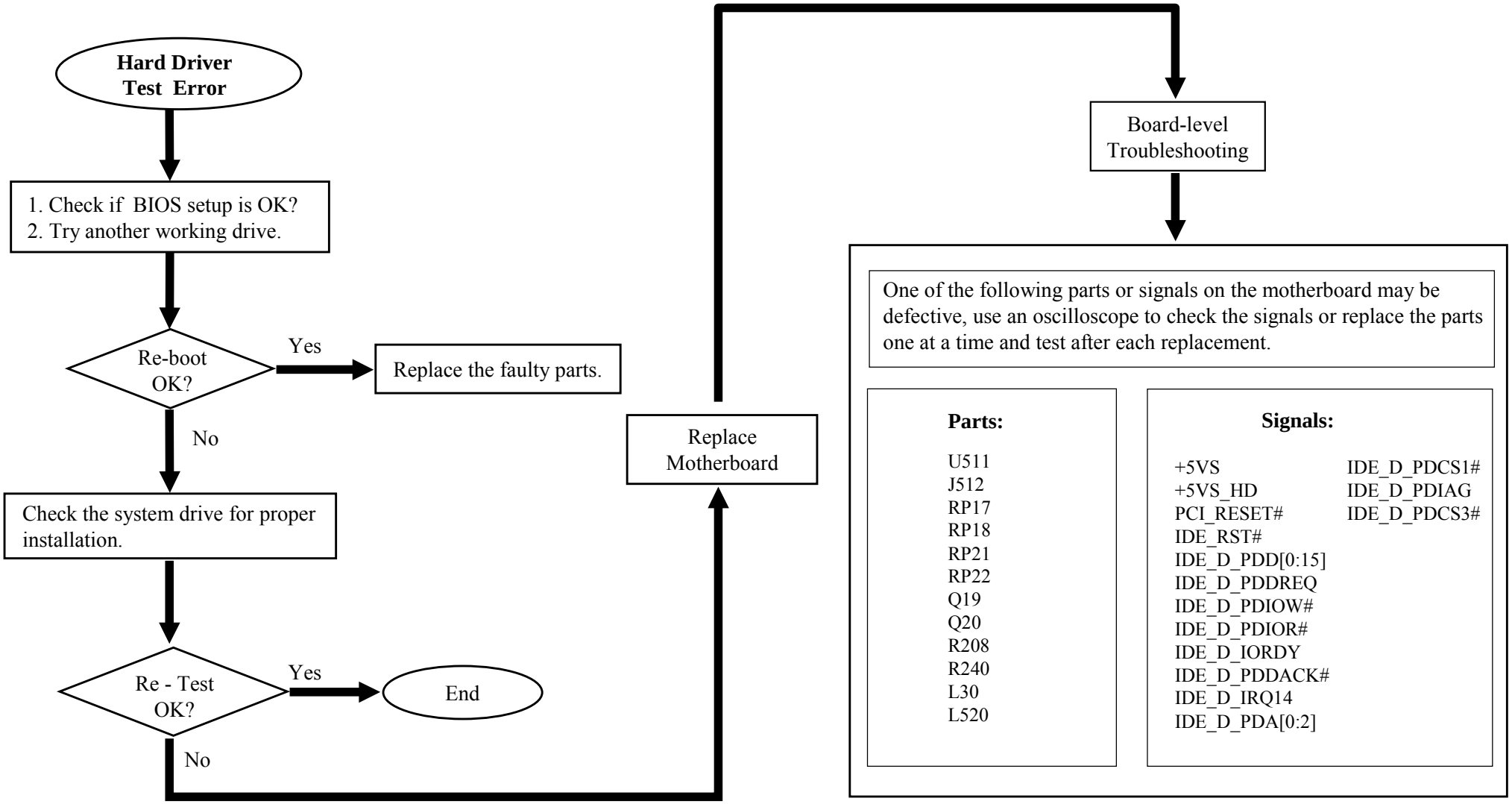
## 8.8 Keyboard (K/B) Touch-Pad (T/P) Test Error (2)

**Error message of keyboard or touch-pad failure is shown or any key does not work.**



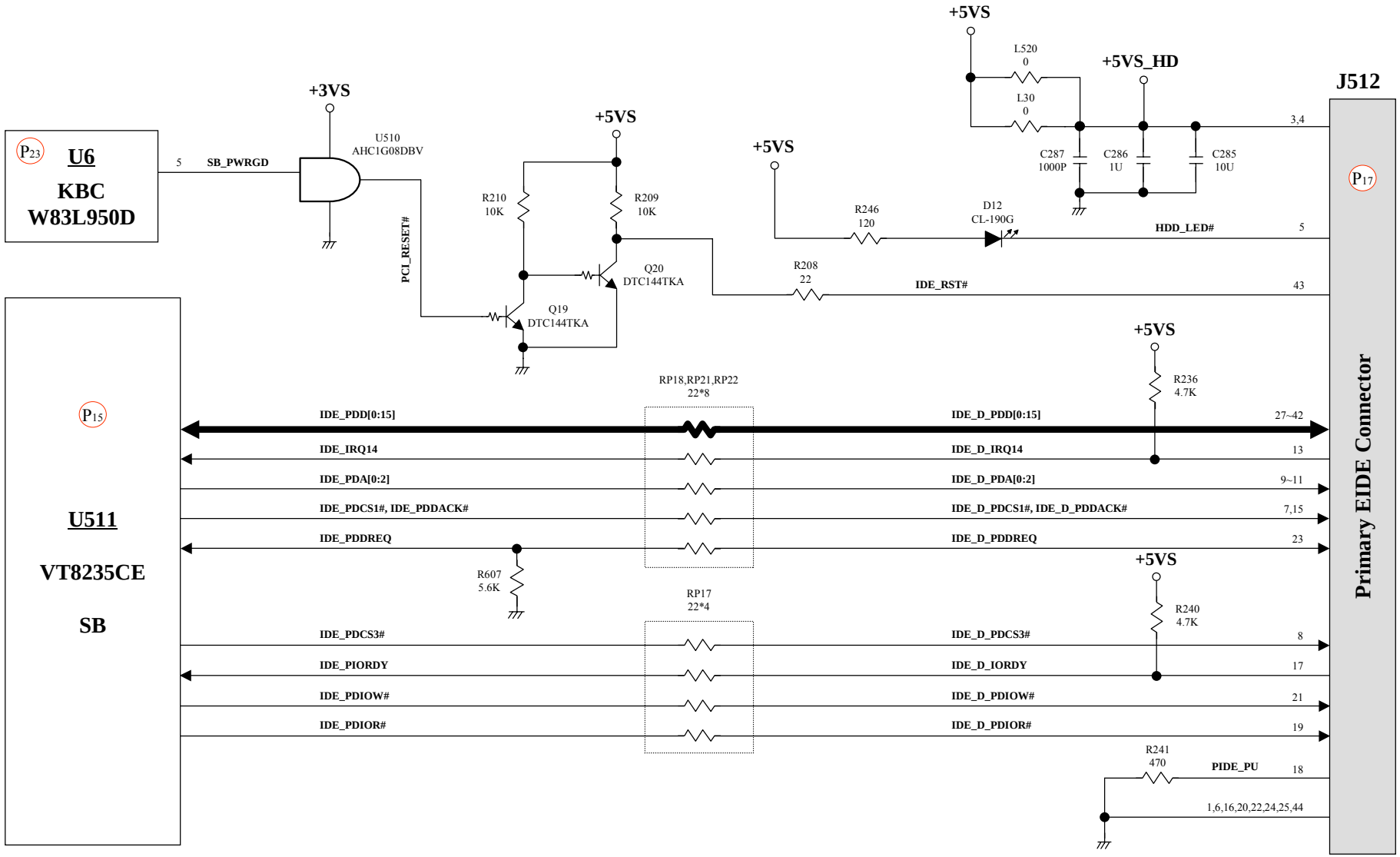
## 8.9 Hard Drive Test Error (1)

**Either an error message is shown, or the driver motor continues spinning, while reading data is from or writing data is to hard drive.**



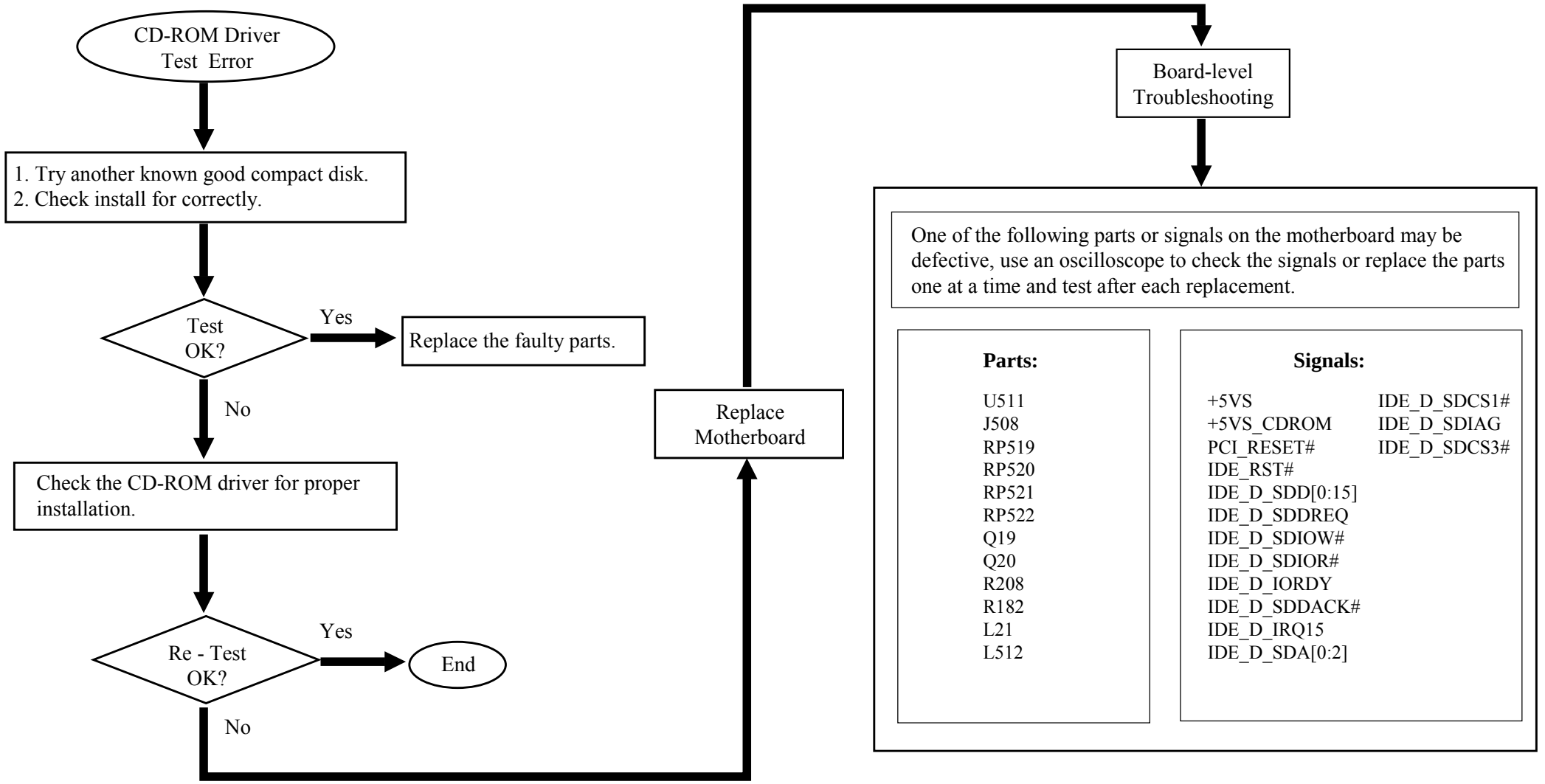
## 8.9 Hard Drive Test Error (2)

**Either an error message is shown, or the driver motor continues spinning, while reading data is from or writing data is to hard drive.**



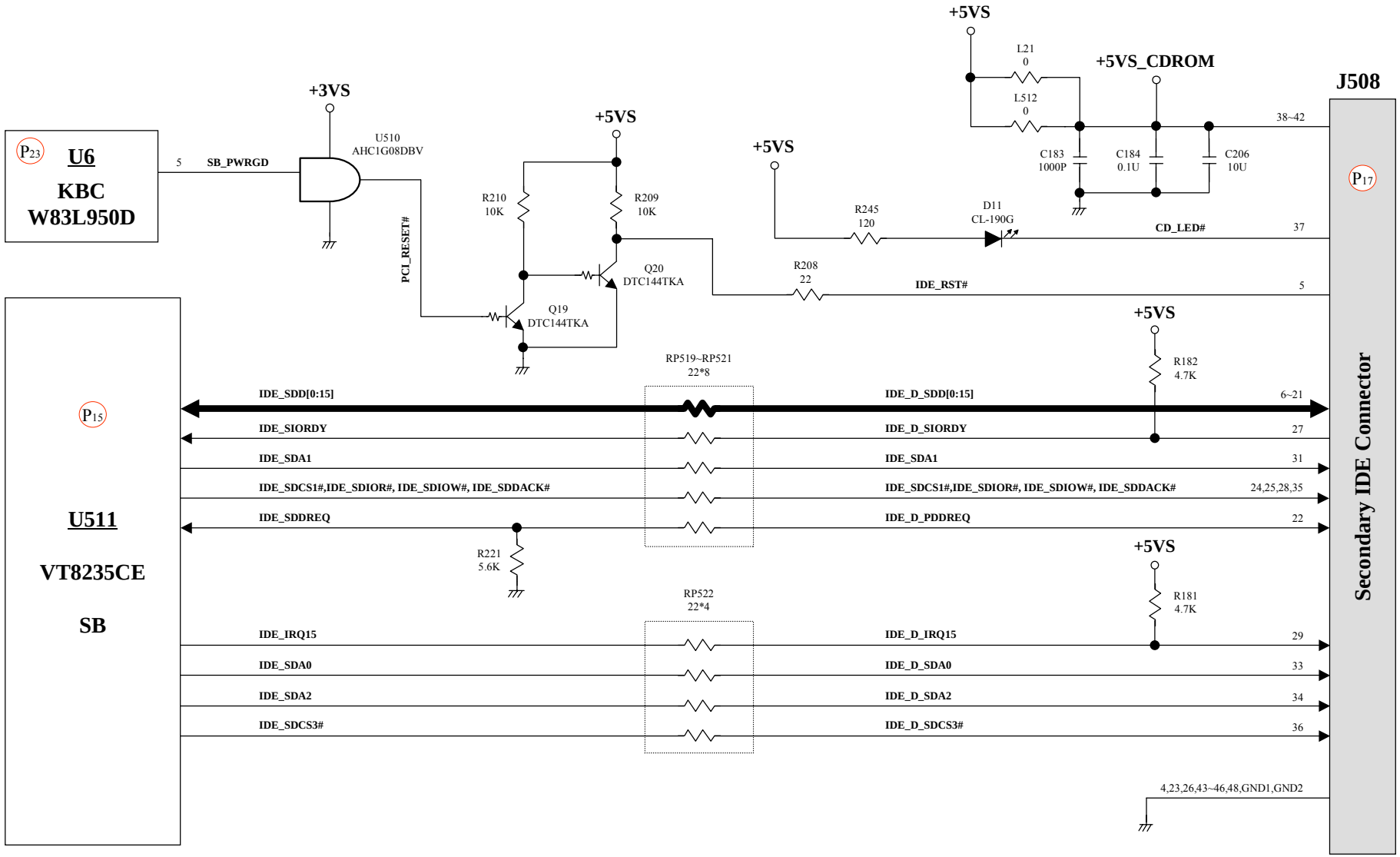
## 8.10 CD-ROM Drive Test Error (1)

**An error message is shown when reading data from CD-ROM drive.**



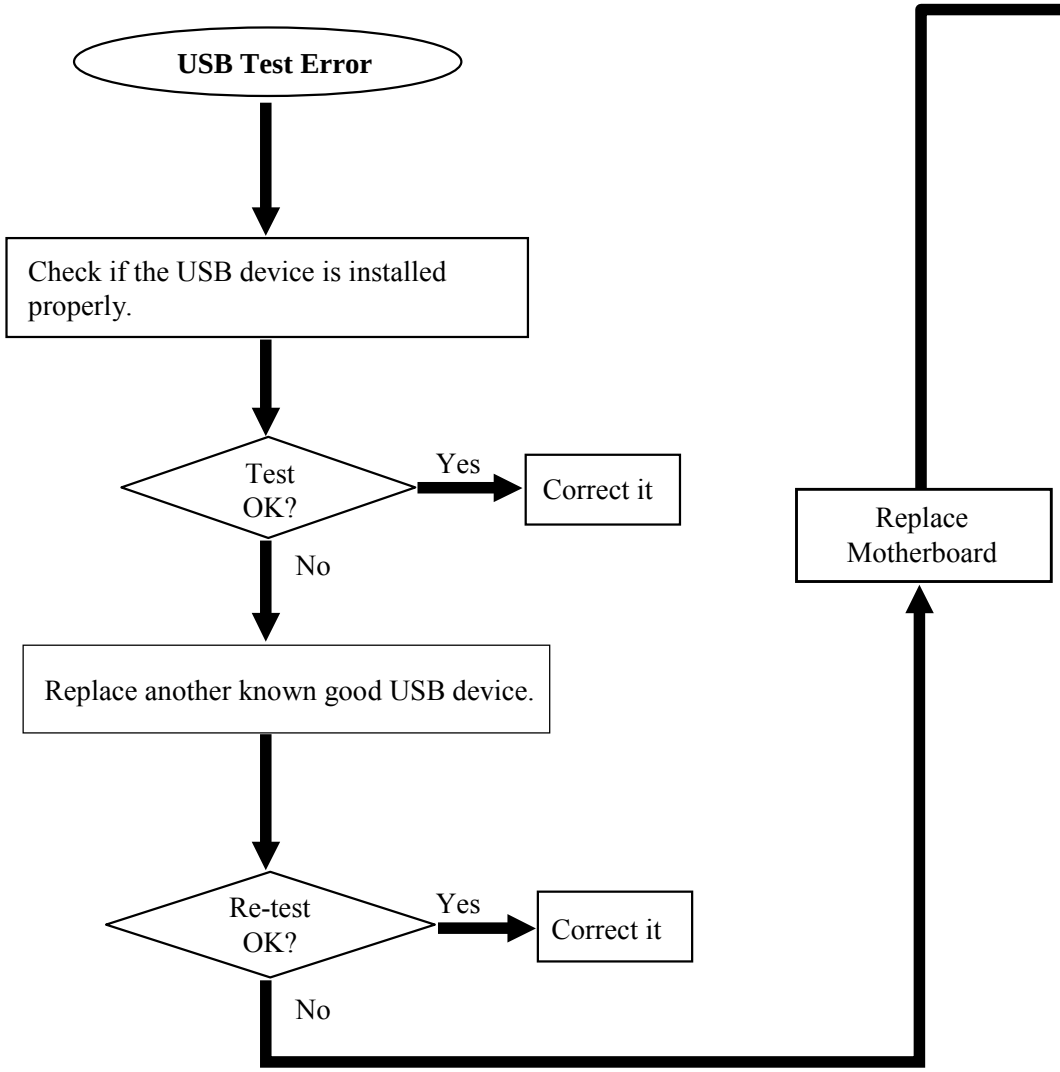
## 8.10 CD-ROM Drive Test Error (2)

**An error message is shown when reading data from CD-ROM drive.**



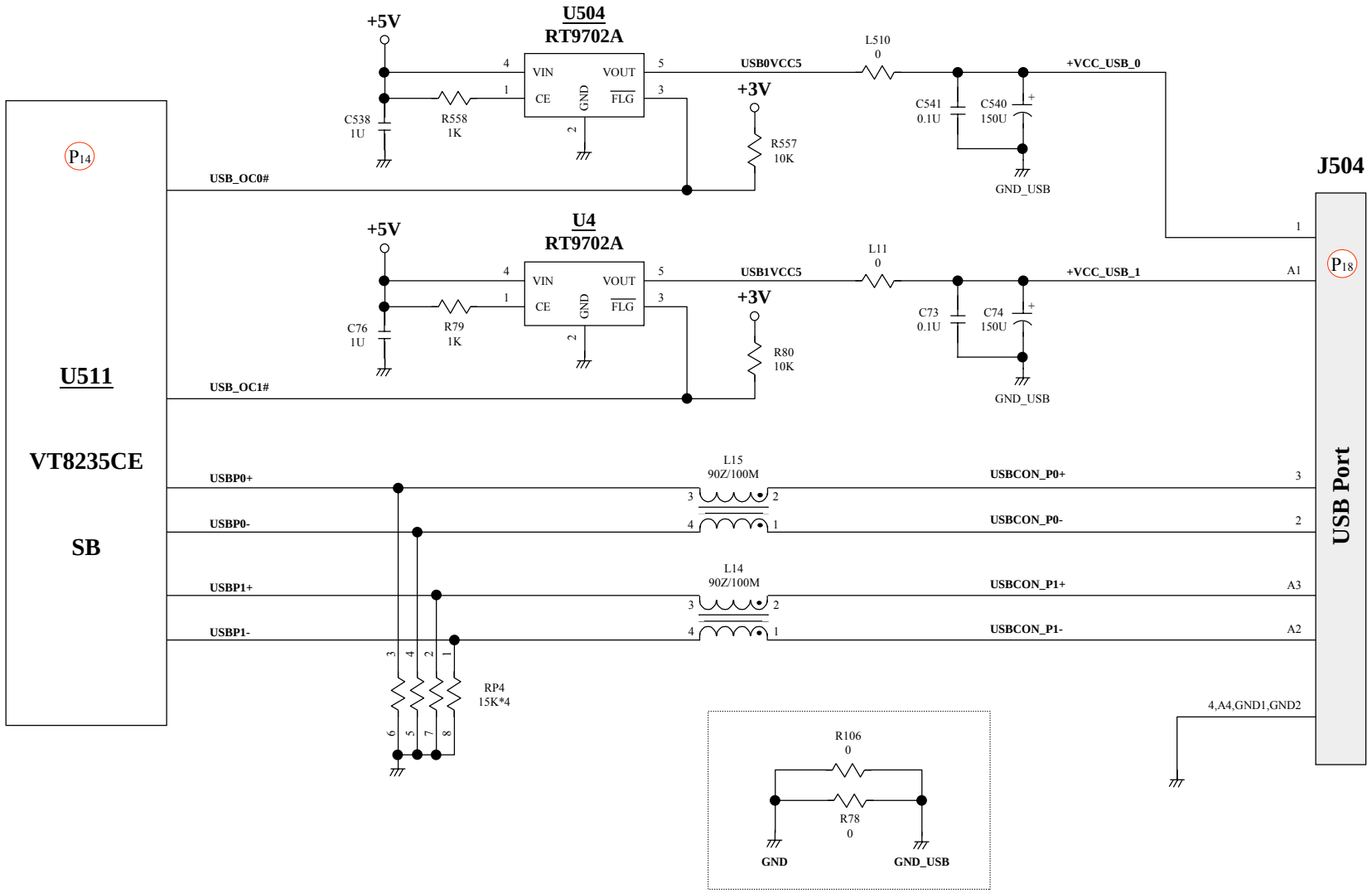
# 8.11 USB Port Test Error (1)

**An error occurs when a USB I/O device is installed.**



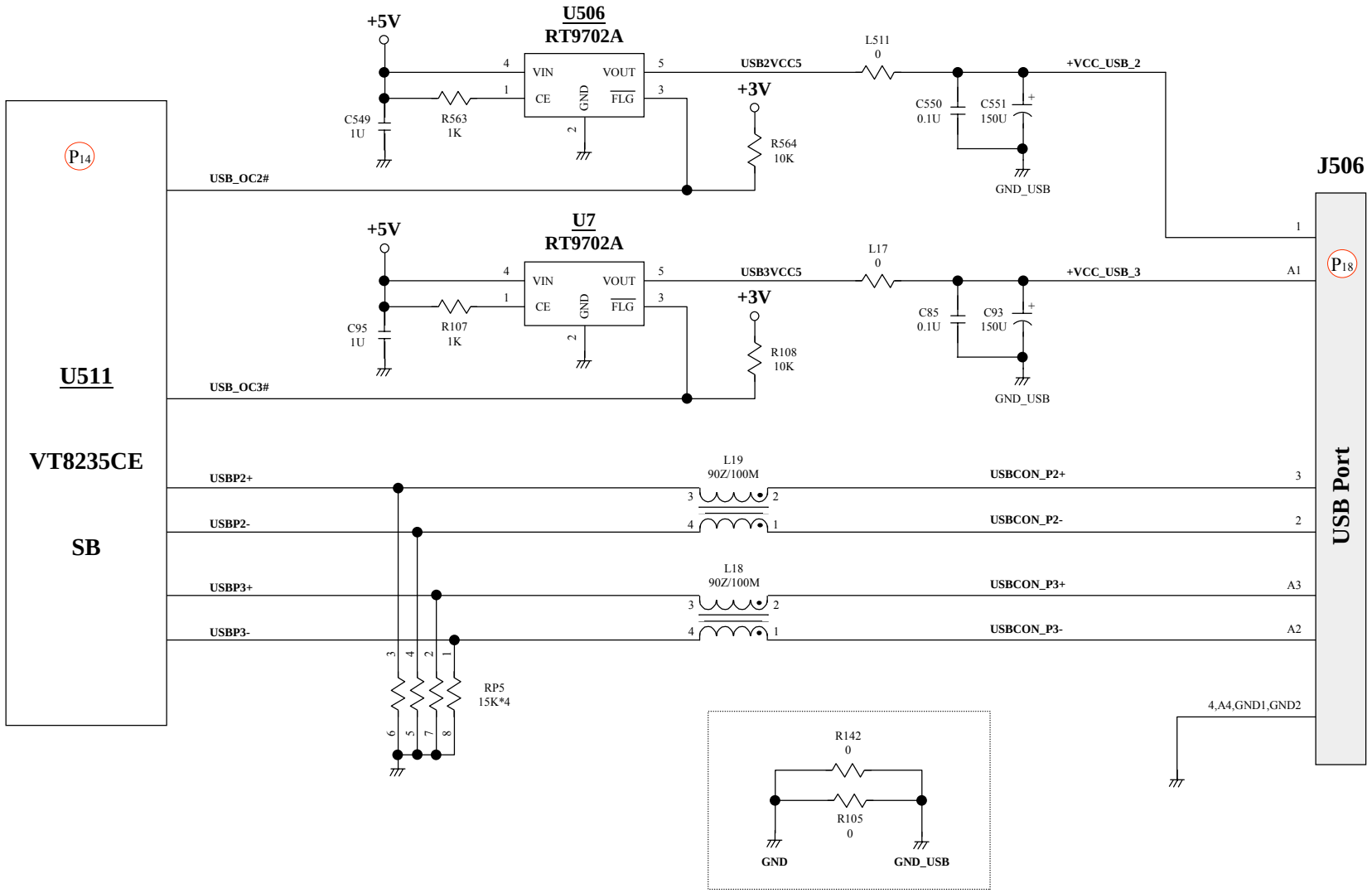
# 8.11 USB Port Test Error (2)

**An error occurs when a USB I/O device is installed.**



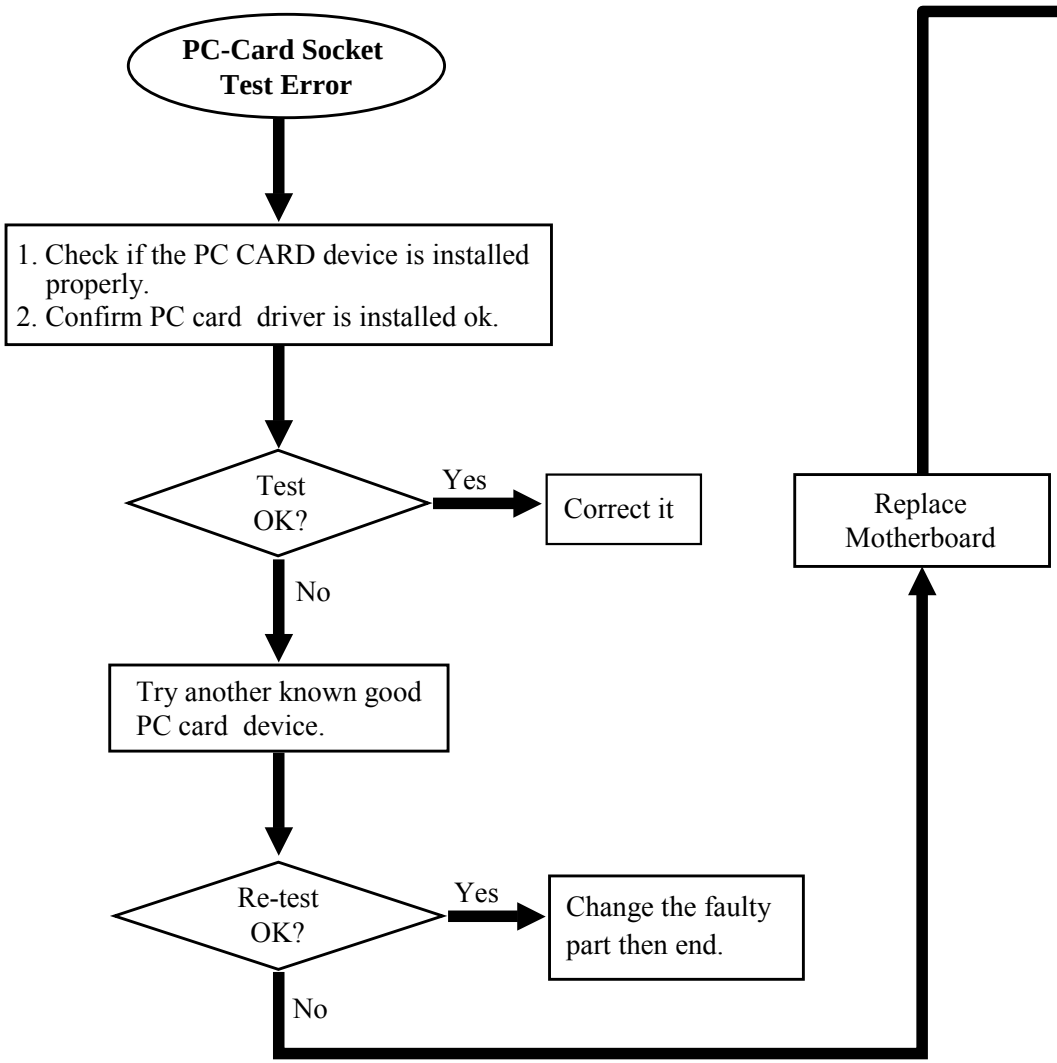
# 8.11 USB Port Test Error (3)

**An error occurs when a USB I/O device is installed.**



# 8.12 PC-Card Socket Test Error (1)

**An error occurs when a PC card device is installed.**




Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

**Parts:**

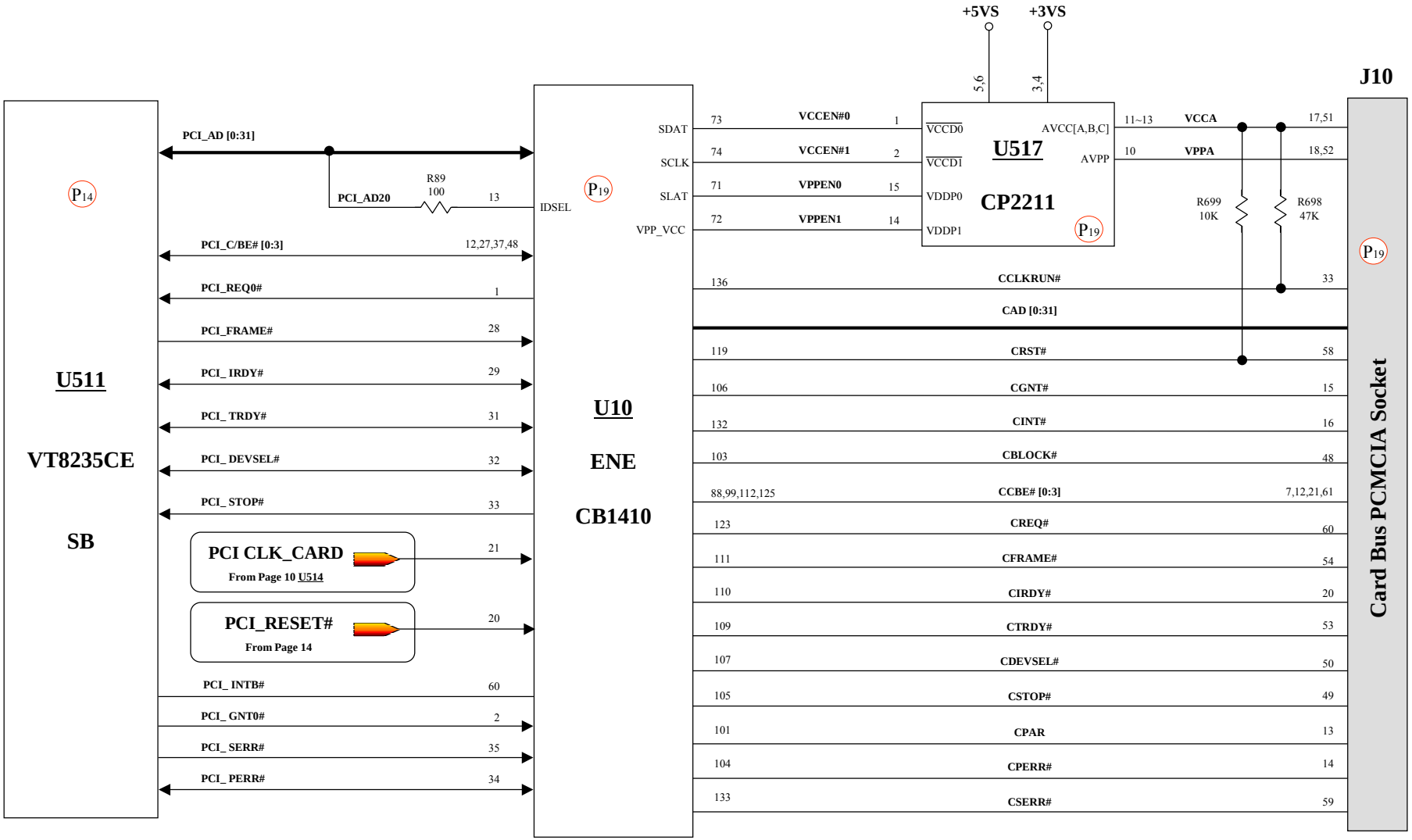
U511
U10
U517
J10
R698
R699
R89
R689
R690
R73

**Signals**

+3VS
VCCA
VPPA
PCI_AD[0:31]
PCI_RESET#
PCI_C/BE#[0:3]
PCI_FRAME#
PCI_IRDY#
PCI_TRDY#
PCI_DEVSEL#
PCI_STOP#
PCI_INTB#
PCI_GNT0#
PCI_SERR#
PCI_PERR#
PCICLK_CARD
PCI_PAR
PCI_REQ0#
CLKRUN#
PCI_LOCK#
SERIRQ

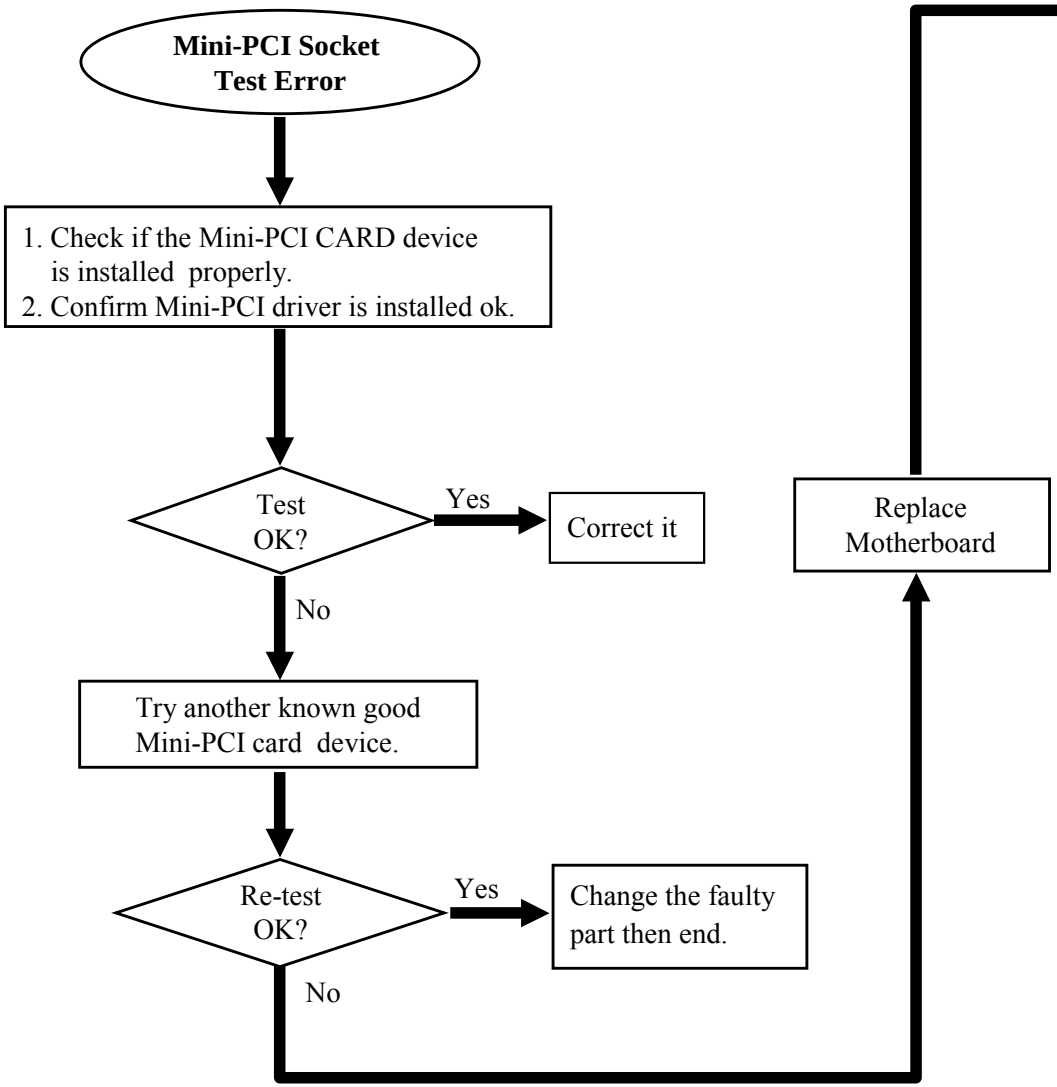
# 8.12 PC-Card Socket Test Error (2)

**An error occurs when a PC card device is installed.**



## 8.13 Mini-PCI Socket Test Error (1)

**An error occurs when a PC card device is installed.**




Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

**Parts:**

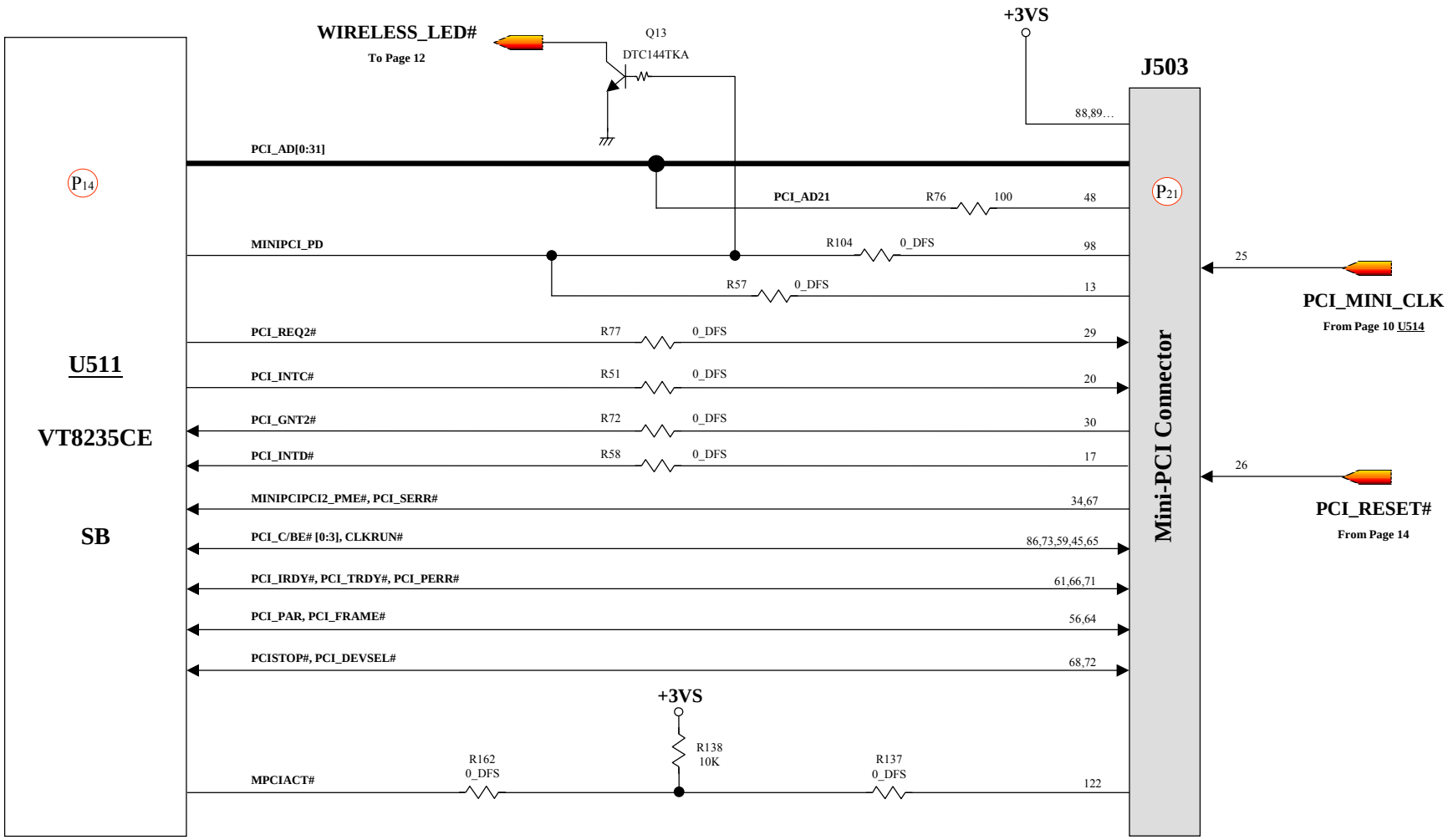
U511
J503
RP3
R57
R58
R77
R51
R72
R76
R104

**Signals**

| | |
|---|---|
| +5VS | PCI_SERR# |
| +3VS | PCI_PERR# |
| PCI_AD[0:31] | PCI_INTD# |
| LPC_LAD[0:3] | PCI_INTC# |
| PCI_C/BE#[0:3] | PCI_RESET# |
| MINIPCI_PD | PCI_GNT2# |
| PCI_INTC# | PCI_PAR |
| PCI_MINI_CLK | PCI_FRAME# |
| PCI_REQ2# | PCI_TRDY# |
| PCI_IRDY# | PCI_STOP# |
| CLKRUN# | PCI_DEVSEL# |

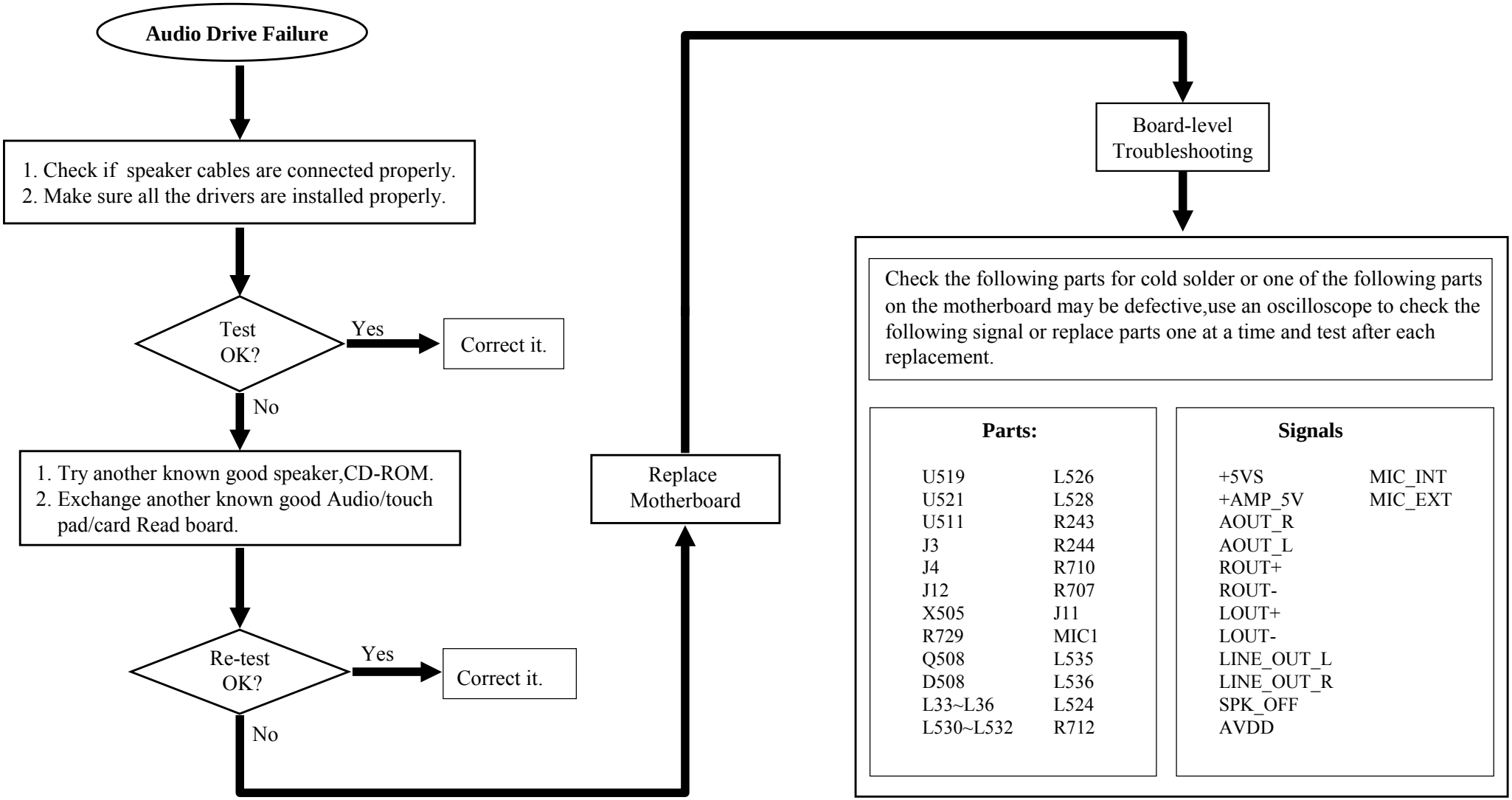
# 8.13 Mini-PCI Socket Test Error (2)

**An error occurs when a PC card device is installed.**



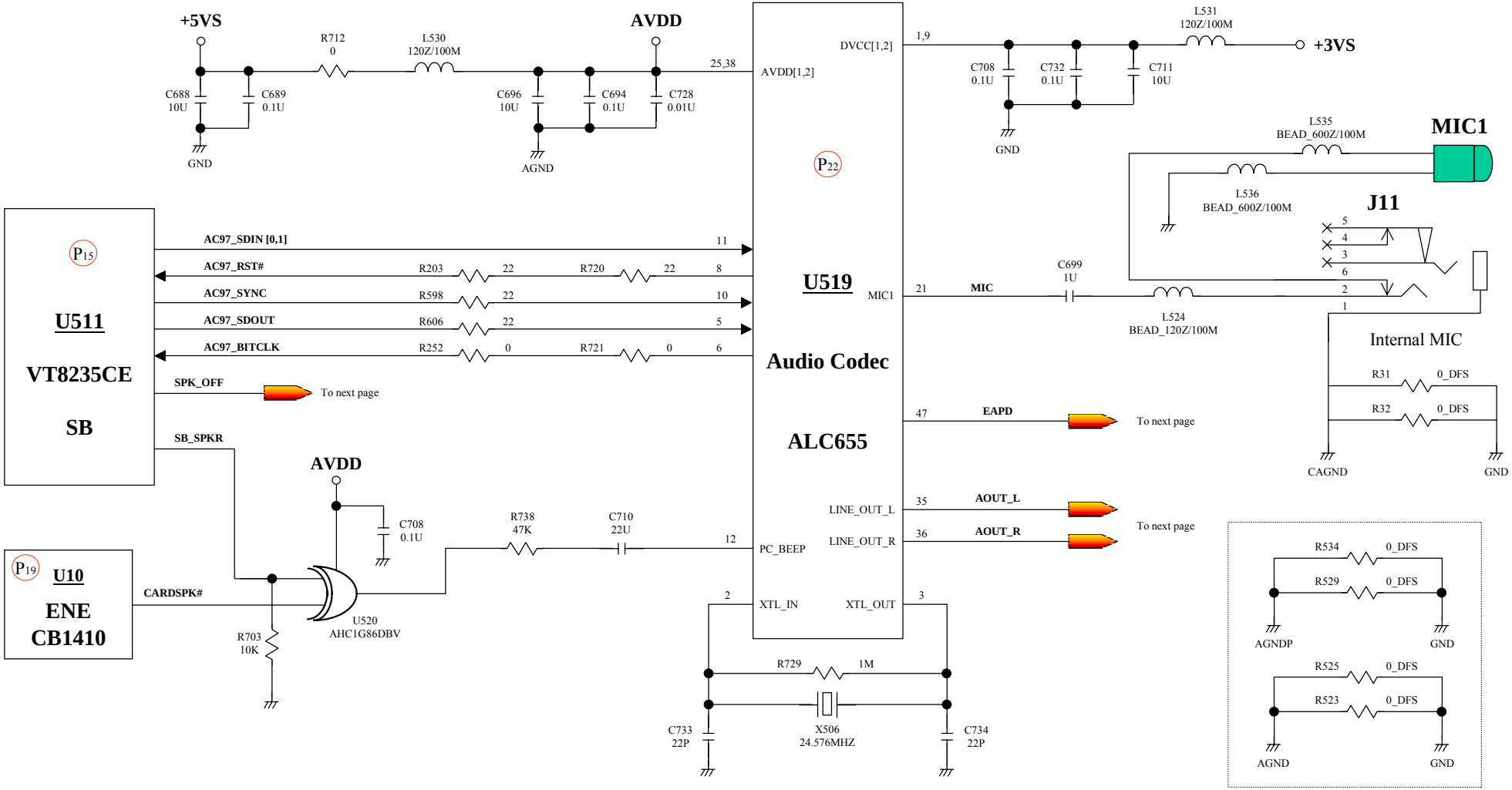
## 8.14 Audio Failure (1)

**No sound from speaker after audio driver is installed.**



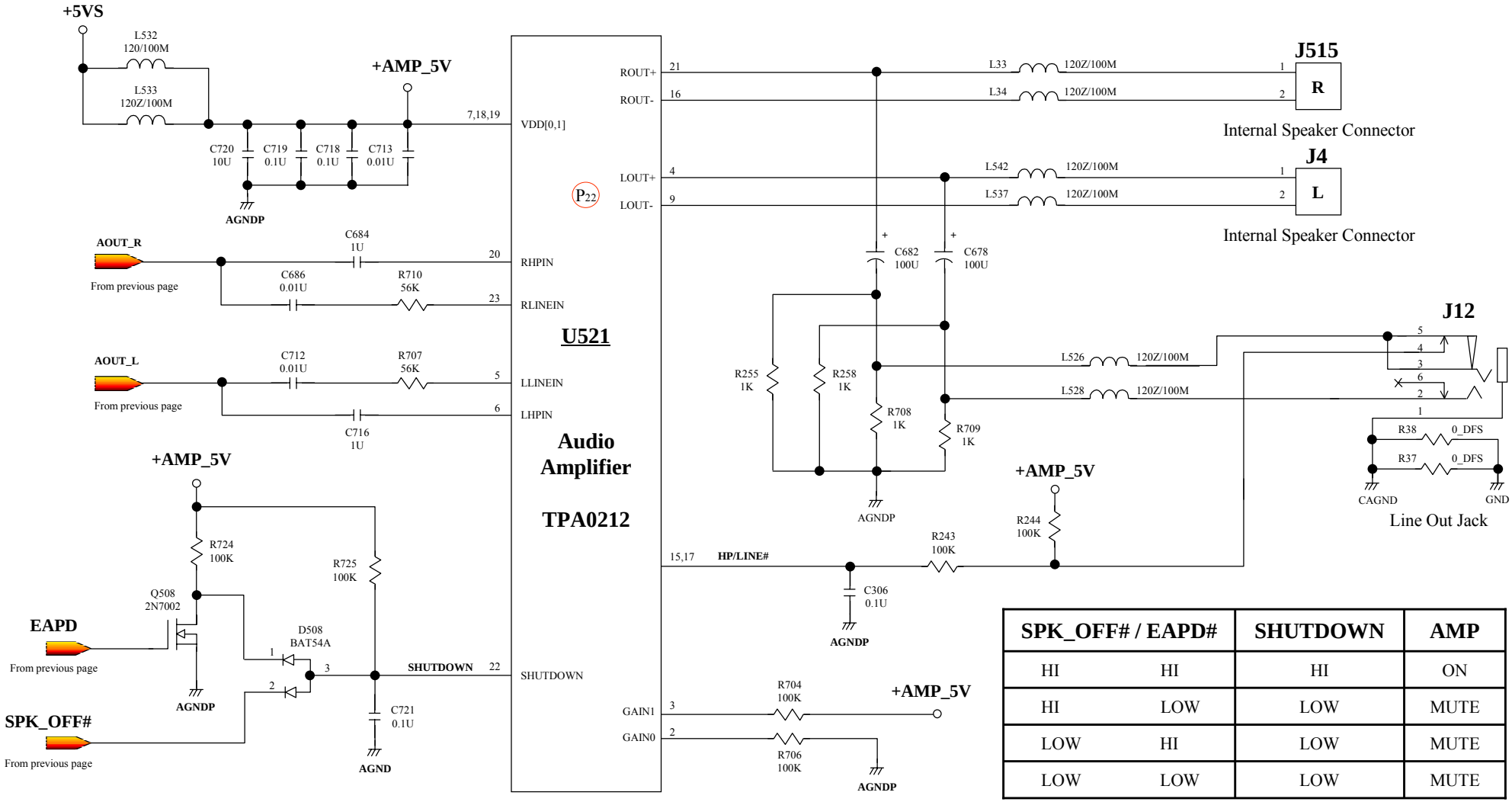
# 8.14 Audio Failure (2) – Audio IN

**No sound from speaker after audio driver is installed.**



# 8.14 Audio Failure (3) – Audio OUT

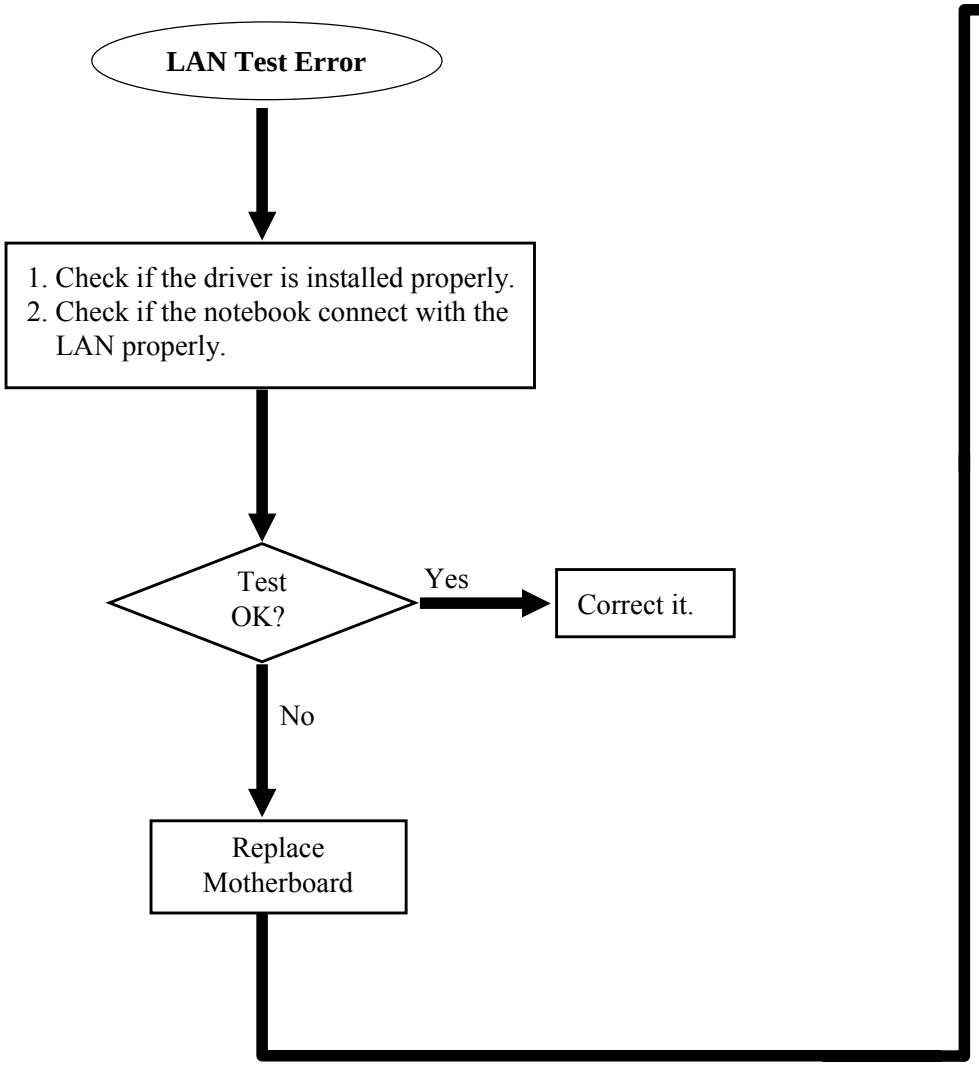
**No sound from speaker after audio driver is installed.**




| SPK_OFF# / EAPD# | | SHUTDOWN | AMP |
|---|---|---|---|
| HI | HI | HI | ON |
| HI | LOW | LOW | MUTE |
| LOW | HI | LOW | MUTE |
| LOW | LOW | LOW | MUTE |

# 8.15 LAN Test Error (1)

**An error occurs when a LAN device is installed.**




Board-level Troubleshooting

Check the following parts for cold solder or one of the following parts on the mother-board may be defective, use an oscilloscope to check the following signal or replace the parts one at a time and test after each replacement.

**Parts:**

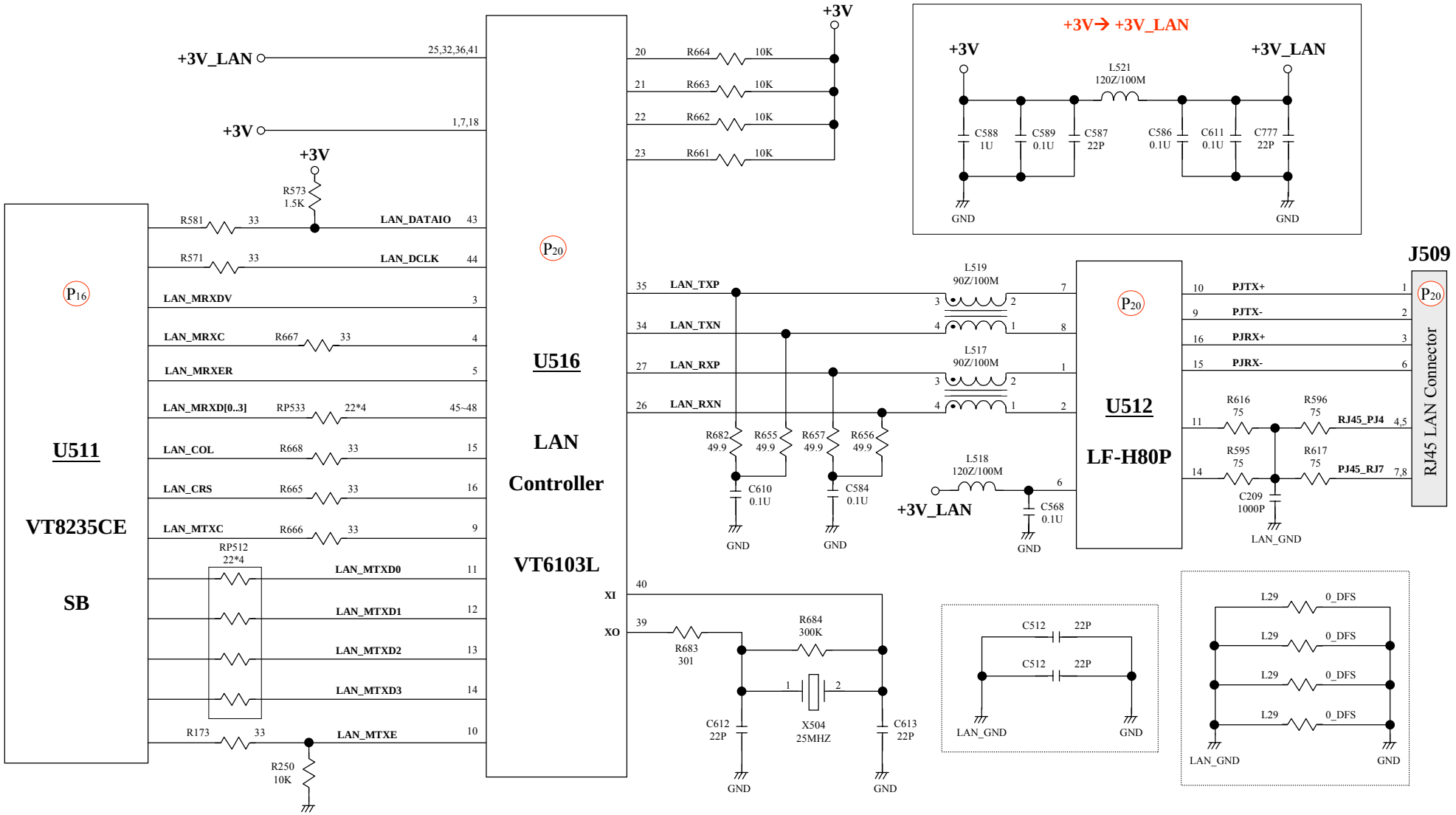
| | |
|---|---|
| U511 | U512 |
| U515 | L517 |
| R173 | L519 |
| RP512 | J509 |
| R573 | R655 |
| L521 | R656 |
| R666 | R657 |
| R665 | R682 |
| R668 | R595 |
| R667 | R596 |
| RP533 | R616 |
| X504 | R617 |

**Signals**

| | |
|---|---|
| +3V | LAN_CRS |
| +3V_LAN | LAN_TXP |
| LAN_MTXD[0:3] | LAN_TXN |
| LAN_MRXD[0:3] | LAN_RXP |
| LAN_MRXDV | LAN_RXN |
| LAN_MRXER | |
| LAN_MRXC | |
| LAN_MTXE | |
| LAN_MTXC | |
| LAN_DCLK | |
| LAN_DADAIO | |
| LAN_COL | |

# 8.15 LAN Test Error (2)

**An error occurs when a LAN device is installed.**



# 9. Spare Parts List (1)

| Part Number | Description | Location(S) |
|---|---|---|
| 221672350007 | REINFORCE BRKT;50 x 50 x 830MM | |
| 221673550007 | REINFORCE BRKT;L985*50*50*T5 | |
| 221674550004 | REINFORCE BRKT;L800*50*50*T5 | |
| 221677040001 | BOX,AK,LYNX | |
| 221677050003 | CARD BOARD;TOP/BTM,PALLET,LYNX | |
| 221682820009 | CARTON;NON-BRAND,8089P | |
| 221682850002 | CARD BOARD;FRAME,PALLET,8089P | |
| 222503220001 | PE BUBBLE BAG;BATTERY,GRAMPUS | |
| 222600020049 | PE BAG;50*70MM,W/SEAL,COMMON | |
| 222600020310 | PE BAG;70X100MM,W/SEAL,COMMON | |
| 222670000001 | PE BUBBLE BAG;BATTERY,7521 | |
| 222670820003 | PE BAG;L560*W345,7521N | |
| 222671330003 | PE BAG;LCD BRACKET,STINGRAY | |
| 222671620001 | PE BUBBLE BAG;CD-ROM HOUSING,817 | |
| 222672730001 | PE BUBBLE BAG;200*240mm,AMM-9019 | |
| 224672330001 | PALLET;1200x1050x135MM,MANGUSTA | |
| 225600000054 | TAPE;INSULATING,POLYESTER FILM,1 | |
| 225600000061 | TAPE;ADHENSIVE,DOUBLE-FACE,W20,U | |
| 226600030332 | SPONGE;320*290*10,CAIMAN,PWR | |
| 227677000001 | END CAP;L/R,LYNX | |
| 227677000002 | PAD;LCD/KB,LYNX | |
| 242600000145 | LABEL;10*10,BLANK,COMMON | |
| 242600000145 | LABEL;10*10,BLANK,COMMON | |
| 242600000157 | LABEL;BAR CODE,125*65,COMMON | |
| 242600000439 | LABEL;25*6,HI-TEMP,COMMON | |

| Part Number | Description | Location(S) |
|---|---|---|
| 242664800013 | LABEL;CAUTION,INVERT BD,PITCHING | |
| 242669600005 | LABEL;LOT NUMBER,RACE | |
| 242670800113 | BFM-WORLD MARK;WINXP,7521N | |
| 242677000027 | LABEL,AK BOX,LYNX | |
| 242679900005 | LABEL;BAR CODE,(25*10MM)*12pcs,8 | |
| 242685200005 | LABEL;BATT,11.1V/6.0AH,LI,PANASO | |
| 242685200010 | LABEL;N-B,AGENCY-GLOBAL,8889 | |
| 270140000003 | VARISTOR;280V,5.6X3.8MM,TVB280-0 | S501 |
| 271002000301 | RES;0 ,1/10W,5% ,0805,SMT | R251,R501,R712,R736,R741 |
| 271002472301 | RES;4.7K ,1/10W,5% ,0805,SMT | PR505,PR506 |
| 271002478301 | RES;4.7 ,1/10W,5% ,0805,SMT | PR37,PR516,PR523 |
| 271002614101 | RES;619K ,1/10W,1% ,0805,SMT | PR36 |
| 271012221301 | RES;220 ,1/8W,5% ,1206,SMT | PR13,PR3 |
| 271045107101 | RES;.01 ,1W ,1% ,2512,SMT | PR507,PR510 |
| 271045507101 | RES;.05 ,1W ,1% ,2512,SMT | PR511 |
| 271046407101 | RES;.040 ,2W ,1% ,2512,SMT,PRC | R18A,R18B,R18C |
| 271061000002 | RES;0 ,1/16W,0402,SMT | PR107,PR19,PR59,PR71,PR72,PR |
| 271061101103 | RES;100 ,1/16W,1% ,0402,SMT | R147,R148,R597,R60,R76,R89 |
| 271061102105 | RES;1K ,1/16W,1% ,0402,SMT | R545,R548,R549 |
| 271061102303 | RES;1K ,1/16W,5% ,0402,SMT | PR11,PR39,PR52,PR526,PR529,P |
| 271061103501 | RES;10K ,1/16W,5% ,0402,SMT | PR111,PR112,PR113,R100,R108,I |
| 271061104102 | RES;100K ,1/16W,1% ,0402,SMT | PR525 |
| 271061104501 | RES;100K ,1/16W,5% ,0402,SMT | PR101,PR102,PR106,PR110,PR21 |
| 271061105501 | RES;1M ,1/16W,5% ,0402,SMT | PR22,PR98,R553,R601,R603,R729 |
| 271061106501 | RES;10M ,1/16W,5% ,0402,SMT | R624 |

# 9. Spare Parts List (2)

| Part Number | Description | Location(S) |
|---|---|---|
| 271061121501 | RES;120 ,1/16W,5% ,0402,SMT | R152,R163,R164,R167,R245,R246 |
| 271061152302 | RES;15K ,1/16W,5% ,0402,SMT | R228 |
| 271061152501 | RES;1.5K ,1/16W,5% ,0402,SMT | R573 |
| 271061154501 | RES;150K ,1/16W,5% ,0402,SMT | R555 |
| 271061203102 | RES;20K ,1/16W,1% ,0402,SMT | PR28 |
| 271061220501 | RES;22 ,1/16W,5% ,0402,SMT | R140,R141,R203,R208,R28,R29,R |
| 271061222501 | RES;2.2K ,1/16W,5% ,0402,SMT | R217,R218,R220,R513,R519,R521 |
| 271061301112 | RES;301 ,1/16W,1% ,0402,SMT | R683 |
| 271061302101 | RES;3K ,1/16W,1% ,0402,SMT | R65 |
| 271061324211 | RES;32.4K,1/16W,1% ,0402,SMT | PR524 |
| 271061330501 | RES;33 ,1/16W,5% ,0402,SMT | PR520,R173,R571,R581,R665,R66 |
| 271061361101 | RES;360 ,1/16W,1% ,0402,SMT | R183,R195,R586,R64 |
| 271061464112 | RES;4.64K ,1/16W,1% ,0402,SMT | R22 |
| 271061470501 | RES;47 ,1/16W,5% ,0402,SMT | R165,R168,R169,R264,R265,R266 |
| 271061471501 | RES;470 ,1/16W,5% ,0402,SMT | R241 |
| 271061472102 | RES;4.7K ,1/16W,1% ,0402,SMT | R184 |
| 271061472501 | RES;4.7K ,1/16W,5% ,0402,SMT | R12,R13,R176,R177,R178,R179,R |
| 271061473102 | RES;47K ,1/16W,1% ,0402,SMT | PR519,PR522,R707,R710 |
| 271061473501 | RES;47K ,1/16W,5% ,0402,SMT | R698,R738 |
| 271061474501 | RES;470K ,1/16W,5% ,0402,SMT | R618,R623 |
| 271061475211 | RES;4.75K,1/16W,1% ,0402,SMT | PR1 |
| 271061499012 | RES;49.9 ,1/16W,1% ,0402,SMT | R591,R592,R61,R62,R655,R656,R |
| 271061562501 | RES;5.6K ,1/16W,5% ,0402,SMT | R221,R607 |
| 271061604011 | RES;60.4 ,1/16W,1% ,0402,SMT | R525,R526 |
| 271061649212 | RES;6.49K,1/16W,1% ,0402,SMT | R658 |

| Part Number | Description | Location(S) |
|---|---|---|
| 271061681501 | RES;680 ,1/16W,5% ,0402,SMT | R113,R114,R115,R122,R128,R129 |
| 271061753101 | RES;75,1/16W,1%,0402,SMT | R247,R248,R249,R595,R596,R616 |
| 271061821302 | RES;820 ,1/16W,5% ,0402,SMT | R118,R119 |
| 271061862101 | RES;8.66K ,1/16W,1% ,0402,SMT | PR103 |
| 271071000002 | RES;0 ,1/16W,5% ,0603,SMT | PR16,PR17,PR18,PR45,PR514,PR |
| 271071010301 | RES;1 ,1/16W,5% ,0603,SMT | PR108,PR109,PR31,PR34 |
| 271071100302 | RES;10 ,1/16W,5% ,0603,SMT | PR530,PR74 |
| 271071101301 | RES;100 ,1/16W,5% ,0603,SMT | PR47 |
| 271071101301 | RES;100 ,1/16W,5% ,0603,SMT | R37 |
| 271071102102 | RES;1K ,1/16W,1% ,0603,SMT | PR70 |
| 271071102302 | RES;1K ,1/16W,5% ,0603,SMT | R11 |
| 271071102302 | RES;1K ,1/16W,5% ,0603,SMT | PR63,PR64,PR65,PR66,PR80 |
| 271071102302 | RES;1K ,1/16W,5% ,0603,SMT | R35,R39,R43 |
| 271071103101 | RES;10K ,1/16W,1% ,0603,SMT | PR91 |
| 271071103302 | RES;10K ,1/16W,5% ,0603,SMT | PR20,PR77,PR99 |
| 271071103302 | RES;10K ,1/16W,5% ,0603,SMT | R3,R4 |
| 271071104101 | RES;100K ,1/16W,1% ,0603,SMT | PR32,PR38,PR41,PR42,PR48,PR5 |
| 271071104101 | RES;100K ,1/16W,1% ,0603,SMT | R7 |
| 271071104302 | RES;100K ,1/16W,5% ,0603,SMT | R7 |
| 271071104302 | RES;100K ,1/16W,5% ,0603,SMT | PR25,PR44,PR504,PR53,PR54 |
| 271071104302 | RES;100K ,1/16W,5% ,0603,SMT | R11,R15,R2,R38,R44,R48 |
| 271071105301 | RES;1M ,1/16W,5% ,0603,SMT | PR503,PR528,PR90 |
| 271071105301 | RES;1M ,1/16W,5% ,0603,SMT | R40 |
| 271071107311 | RES;107K ,1/16W,1% ,0603,SMT | PR5 |
| 271071113101 | RES;11K ,1/16W,1% ,0603,SMT | PR89 |

# 9. Spare Parts List (3)

| Part Number | Description | Location(S) |
|---|---|---|
| 271071113113 | RES;1.13K,1/16W,1%,0603,SMT | PR8 |
| 271071114101 | RES;110K ,1/16W,1% ,0603,SMT | PR79 |
| 271071121211 | RES;12.1K,1/16W,1% ,0603,SMT | PR50 |
| 271071134101 | RES;130K ,1/16W,1% ,0603,SMT | PR35 |
| 271071137011 | RES;137 ,1/16W,1% ,0603,SMT | R14A |
| 271071137211 | RES;13.7K,1/16W,1% ,0603,SMT | PR33 |
| 271071151101 | RES;150 ,1/16W,1% ,0603,SMT | R36,R48 |
| 271071151103 | RES;15 ,1/16W,1% ,0603,SMT | R647,R648 |
| 271071152302 | RES;1.5K ,1/16W,5% ,0603,SMT | R17 |
| 271071152302 | RES;1.5K ,1/16W,5% ,0603,SMT | R19 |
| 271071153101 | RES;15K ,1/16W,1% ,0603,SMT | PR518 |
| 271071169011 | RES;169 ,1/16W,1% ,0603,SMT | R562 |
| 271071169111 | RES;1.69K,1/16W,1% ,0603,SMT | PR58 |
| 271071201301 | RES;200 ,1/16W,5% ,0603,SMT | R14,R17 |
| 271071202102 | RES;2K ,1/16W,1% ,0603,SMT | PR57 |
| 271071202301 | RES;2K ,1/16W,5% ,0603,SMT | R12 |
| 271071203101 | RES;20K ,1/16W,1% ,0603,SMT | PR14,PR4,PR7 |
| 271071220101 | RES;22 ,1/16W,1% ,0603,SMT | R517,R518,R83 |
| 271071225301 | RES;2.2M,1/16W,5% ,0603,SMT | R34,R36 |
| 271071226311 | RES;226K ,1/16W,1% ,0603,SMT | PR26 |
| 271071244301 | RES;240K ,1/16W,5% ,0603,SMT | R41 |
| 271071301311 | RES;301K ,1/16W,1% ,0603,SMT | R13,R3 |
| 271071304301 | RES;300K ,1/16W,5% ,0603,SMT | R684 |
| 271071304301 | RES;300K ,1/16W,5% ,0603,SMT | R42 |
| 271071324111 | RES;3.24K,1/16W,1% ,0603,SMT | PR62 |

| Part Number | Description | Location(S) |
|---|---|---|
| 271071330103 | RES;33.2,1/16W,1%,0603,SMT | R82 |
| 271071331301 | RES;330 ,1/16W,5% ,0603,SMT | R16,R20,R22 |
| 271071331301 | RES;330 ,1/16W,5% ,0603,SMT | R18,R21,R23 |
| 271071333301 | RES;33K ,1/16W,5% ,0603,SMT | PR27 |
| 271071342101 | RES;3.4K ,1/16W,1% ,0603,SMT | PR49 |
| 271071362101 | RES;3.6K ,1/16W,1% ,0603,SMT | PR75,PR76 |
| 271071422211 | RES;42.2K,1/16W,1% ,0603,SMT | PR96 |
| 271071432111 | RES;4.32K,1/16W,1% ,0603,SMT | R10 |
| 271071432211 | RES;43.2K,1/16W,1% ,0603,SMT | R1 |
| 271071442113 | RES;44.2 ,1/16W,1% ,0603,SMT | R153,R154,R95,R96 |
| 271071442211 | RES;44.2K,1/16W,1% ,0603,SMT | PR51 |
| 271071471302 | RES;470 ,1/16W,5% ,0603,SMT | PR95 |
| 271071471302 | RES;470 ,1/16W,5% ,0603,SMT | R1 |
| 271071472101 | RES;4.7K ,1/16W,1% ,0603,SMT | PR517 |
| 271071473101 | RES;47K ,1/16W,1% ,0603,SMT | PR508,PR509 |
| 271071473301 | RES;47K ,1/16W,5% ,0603,SMT | PR527,PR67 |
| 271071474301 | RES;470K ,1/16W,5% ,0603,SMT | PR501 |
| 271071475011 | RES;475 ,1/16W,1% ,0603,SMT | PR60 |
| 271071475211 | RES;47.5K,1/16W,1% ,0603,SMT | PR69 |
| 271071499111 | RES;4.99K,1/16W,1% ,0603,SMT | PR15 |
| 271071499311 | RES;499K ,1/16W,1% ,0603,SMT | PR512,PR85,PR86 |
| 271071511211 | RES;51.1K,1/16W,1% ,0603,SMT | PR43 |
| 271071512101 | RES;5.1K ,1/16W,1% ,0603,SMT | R172 |
| 271071513101 | RES;51K ,1/16W,1% ,0603,SMT | PR68 |
| 271071562301 | RES;5.6K ,1/16W,5% ,0603,SMT | R45 |

# 9. Spare Parts List (4)

| Part Number | Description | Location(S) |
|---|---|---|
| 271071563101 | RES;56K ,1/16W,1% ,0603,SMT | R6 |
| 271071563101 | RES;56K ,1/16W,1% ,0603,SMT | PR61 |
| 271071634211 | RES;63.4K,1/16W,1% ,0603,SMT | PR12 |
| 271071665011 | RES;665 ,1/16W,1% ,0603,SMT | R185 |
| 271071698311 | RES;698K ,1/16W,1% ,0603,SMT | R5 |
| 271071751101 | RES;750 ,1/16W,1% ,0603,SMT | R171 |
| 271071753301 | RES;75K ,1/16W,5% ,0603,SMT | R8 |
| 271071806111 | RES;8.06K,1/16W,1% ,0603,SMT | PR2 |
| 271071806211 | RES;80.6K,1/16W,1% ,0603,SMT | PR521 |
| 271071806812 | RES;80.6 ,1/16W,1% ,0603,SMT | R561 |
| 271071822102 | RES;8.2K ,1/16W,1% ,0603,SMT | R14B |
| 271071825012 | RES;825,1/16W,1%,0603,SMT | R263 |
| 271071900101 | RES;90.9,1/16W,1%,0603,SMT | R31 |
| 271072474101 | RES;470K ,1/10W,1% ,0603,SMT | R4 |
| 271072474101 | RES;470K ,1/10W,1% ,0603,SMT | R5 |
| 271571100301 | RP;10*8 ,16P ,1/16W,5% ,1606,SM | RP10,RP11,RP12,RP13,RP14,RP1 |
| 271571220301 | RP;22*8 ,16P ,1/16W,5% ,1606,SM | RP18,RP21,RP22,RP519,RP520,R |
| 271571470301 | RP;47*8 ,16P ,1/16W,5% ,1606,SM | RP23,RP24,RP25,RP26 |
| 271571680302 | RP; 68*8 ,16P,1/16W,5% ,1606,SM | RP523,RP524,RP525,RP526,RP52 |
| 271586026101 | RES;.02 ,2W,1%,2512,SMT | PR502 |
| 271611103301 | RP;10K*4 ,8P ,1/16W,5% ,0612,SMT | RP20,RP518 |
| 271611153301 | RP;15K*4 ,8P ,1/16W,5% ,0612,SMT | RP4,RP5,RP6 |
| 271611220301 | RP;22*4 ,8P ,1/16W,5% ,0612,SMT | RP17,RP502,RP503,RP504,RP505 |
| 271611330301 | RP;33*4 ,8P ,1/16W,5% ,0612,SMT | RP509 |
| 271611472301 | RP;4.7K*4,8P ,1/16W,5% ,0612,SMT | RP19 |

| Part Number | Description | Location(S) |
|---|---|---|
| 271611750301 | RP;75*4 ,8P ,1/16W,5% ,0612,SMT | RP1,RP501 |
| 271621472302 | RP;4.7K*8,10P,1/32W,5% ,1206,SMT | RP510,RP511 |
| 272001105403 | CAP;1U ,10%,10V ,0805,X7R,SMT | PC80,PC81,PC90,PC91 |
| 272001106702 | CAP;10U,6.3V,+- 20%,0805,X5R,SMT | C10,C119,C122,C132,C142,C145,( |
| 272001106703 | CAP;10U,10V,+80-20%,0805,Y5V,SMT | C16,C20,C200,C203,C206,C217,C |
| 272001475701 | CAP;4.7U ,CR,10V ,+80-20%,0805,Y | C149,C166,C168,C554,C557 |
| 272002225701 | CAP;2.2U ,CR,16V ,+80-20%,0805,Y | C257,PC530 |
| 272002474401 | CAP;.47U ,CR,16V ,10%,0805,X7R,S | C13,C14 |
| 272002475702 | CAP;4.7U ,CR,16V ,+80-20%,Y5V,08 | C2 |
| 272003105701 | CAP;1U ,CR,25V ,+80%-20%,0805, | PC522,PC524,PC525 |
| 272005104402 | CAP;.1U ,50V,+/-10%,0805,X7R,SMT | PC21,PC40,PC521,PC60 |
| 272010680301 | CAP;68P,2KV,5%,1206,NPO,SMT,only | C18 |
| 272010680401 | CAP;68P ,CR,2KV,10%,1206,NPO,SM | |
| 272011106404 | CAP;10U,6.3V,10%,1206,X7R,SMT | PC520,PC59,PC68 |
| 272011226401 | CAP;22U,6.3V,+-20%,1206,X5R,SMT | PC15,PC30 |
| 272012105401 | CAP;1U ,CR,16V ,10%,1206,X7R,S | C14A,C14B |
| 272012105702 | CAP;1U ,CR,16V ,+80-20%,1206,Y | PC64 |
| 272013106701 | CAP;10U ,25V ,+80-20%,1206,Y5U, | PC531,PC533,PC534,PC535,PC53 |
| 272021226701 | CAP;22U ,10V,+80-20%,1210,Y5V,S | PC33,PC35,PC526,PC527,PC528, |
| 272023475401 | CAP;4.7U ,25V ,10%,1210,X5R,SMT | C1 |
| 272023475401 | CAP;4.7U ,25V ,10%,1210,X5R,SMT | PC57 |
| 272030050302 | CAP;5P,3KV,5%,1808,NPO,SMT,only | C19 |
| 272030102401 | CAP;1000P,2KV,10%,1808,X7R,SMT | C209 |
| 272030102405 | CAP;1000P,CR,3KV,10%,1808,X7R,TU | C185,C186 |
| 272071105403 | CAP;1U ,10V ,10%,0603,X5R,SMT | C10,C4 |

# 9. Spare Parts List (5)

| Part Number | Description | Location(S) |
|---|---|---|
| 272071105403 | CAP;1U ,10V ,10%,0603,X5R,SMT | PC106 |
| 272071105701 | CAP;1U ,CR,10V ,80-20%,0603,Y5 | PC529,PC79,PC82 |
| 272071332401 | CAP;.33U ,10V ,10%,0603,X7R,SMT | C2 |
| 272072104402 | CAP;.1U ,CR,16V,10%,0603,X7R,SM | C16,C17,C6 |
| 272072104402 | CAP;.1U ,CR,16V,10%,0603,X7R,SM | C12 |
| 272072104402 | CAP;.1U ,CR,16V,10%,0603,X7R,SM | PC510,PC511,PC86 |
| 272072224402 | CAP;.22U ,16V ,10%,0603,X7R,SMT | PC87,PC92,PC93 |
| 272072224701 | CAP;.22U ,16V ,+80-20%,0603,Y5V, | C130 |
| 272072474701 | CAP;.47U ,16V,+80-20%,0603,Y5V,S | C1,C23,C28 |
| 272073104401 | CAP;.1U ,CR,25V,10%,0603,X7R,PR | C22,C7 |
| 272073151301 | CAP;150P ,CR,25V,5% ,0603,NPO,SM | PC523 |
| 272073223401 | CAP;.022U,CR,25V ,10%,0603,X7R,S | C9 |
| 272073223401 | CAP;.022U,CR,25V ,10%,0603,X7R,S | PC105 |
| 272073332401 | CAP;3300P,CR,25V ,10%,0603,X7R,S | PC75 |
| 272073392401 | CAP;3900P,50V,10%,0603,X7R,SMT | C546,C547 |
| 272073472301 | CAP;4700P,CR,50V ,5% ,0603,X7R,S | C5 |
| 272073682401 | CAP;6800P,CR,25V ,10%,0603,X7R,S | PC74 |
| 272075100401 | CAP;10P ,50V ,10%,0603,COG,SMT | C522,C523,C524 |
| 272075101401 | CAP;100P ,50V ,10%,0603,COG,SMT | C20,C21 |
| 272075101401 | CAP;100P ,50V ,10%,0603,COG,SMT | PC104,PC76,PC78 |
| 272075102403 | CAP;1000P,CR,50V,10%,0603,X7R,SM | PC1,PC10,PC100,PC2,PC48,PC54 |
| 272075103401 | CAP;.01U ,CR,50V ,10%,0603,X7R,S | C11 |
| 272075103401 | CAP;.01U ,CR,50V ,10%,0603,X7R,S | C13,C3,C8 |
| 272075103401 | CAP;.01U ,CR,50V ,10%,0603,X7R,S | PC97 |
| 272075103403 | CAP;.01U ,50V,10%,0603,X7R,SMT | C20,C21,C22 |

| Part Number | Description | Location(S) |
|---|---|---|
| 272075103702 | CAP;.01U ,50V,+80-20%,0603,Y5V,S | PC49,PC501,PC506,PC532,PC540 |
| 272075104703 | CAP;.1U ,50V,+80-20%,0603,Y5V,S | C24,C26,C3,C4,C5,C6 |
| 272075120301 | CAP;12P ,CR,50V ,5% ,0603,NPO,S | C590,C591 |
| 272075152401 | CAP;1500P,CR,50V,10%,0603,X7R,SM | PC12 |
| 272075222401 | CAP;2200P,50V ,10%,0603,X7R,SMT | C15A |
| 272075681401 | CAP;680P ,50V ,10%,0603,X7R,SMT | PC50 |
| 272101015401 | CAP;1U,6.3V,+-10%,0402,X5R,SMT | C12,C129,C527,C528,C564 |
| 272102104401 | CAP;.1U ,CR,10V,10%,0402,X5R,SM | C100,C101,C103,C104,C106,C108 |
| 272102105701 | CAP;1U ,CR,6.3V ,80-20%,0402,Y | C121,C236,C254,C284,C286,C308 |
| 272102224701 | CAP;.22U ,10V ,+80-20%,0402,Y5V, | C105,C107,C109,C111,C112,C139 |
| 272103331401 | CAP;33P ,25V ,+/-10%,0402,NPO,S | C360,C364,C507,C512 |
| 272105100303 | CAP;10P ,CR,50V ,5%,0402,NPO,SM | C113,C114,C117,C141,C143,C144 |
| 272105101401 | CAP;100P ,50V ,5%,0402,COG,SMT | PC20,PC23 |
| 272105102408 | CAP;1000P,CR,50V,10%,0402,X7R,SM | C131,C183,C2,C287,C4,C692,C72 |
| 272105103402 | CAP;.01U ,CR,25V ,10%,0402,X7R,S | C123,C134,C135,C15,C225,C238, |
| 272105103702 | CAP;.01U ,50V,+80-20%,0402,SMT | C686,C712,C713,C728 |
| 272105104701 | CAP;.1U ,16V,+80-20%,0402,SMT | C1,C120,C14,C161,C17,C184,C20 |
| 272105220402 | CAP;22P ,50V ,+ -10%,0402,NPO,S | C102,C118,C311,C312,C313,C314 |
| 272105222501 | CAP;2200P,50V ,+/-20%,0402,X7R,S | C545 |
| 272105271403 | CAP;270P ,50V,+-10%,0402,X7R,SMT | C508,C511,C633,C674 |
| 272105331301 | CAP;330P ,50V,5%,0402,NPO,SMT | C502,C503 |
| 272105332402 | CAP;3300P,50V,10%,0402,SMT | C97 |
| 272431157507 | CAP;150U ,TPC,6.3V,20%,H1.9,7343 | C162,C194,C218,C540,C551,C563 |
| 272431227527 | CAP;220U,4V,+/-20%,H2.8,PT,NCC | PC548,PC549 |
| 272431477508 | CAP;470U,2V5,7343,T520V477M2R5AS | PC107,PC108,PC88 |

# 9. Spare Parts List (6)

| Part Number | Description | Location(S) |
|---|---|---|
| 272601107506 | EC;100U ,6.3V,M,9.3*3.6,-55~105' | C678,C682 |
| 272625470401 | CP;47P*4 ,8P,50V ,10%,1206,NPO,S | CP501,CP510 |
| 272991477501 | CAP ; 470U , 6.3V , 20% , φ8*7. | PC514 |
| 272991687501 | CAP ; 680U , 4V , 20% , φ8*7.7 | PC512 |
| 272993106001 | CAP;10U,25V,2.2mm,X5R,KYOCERA,SM | PC43,PC44,PC507,PC516,PC517, |
| 273000130038 | FERRITE CHIP;600OHM/100MHZ,1608, | L33,L34,L526,L528,L535,L536,L |
| 273000130039 | FERRITE CHIP;130OHM/100MHZ,1608, | L10,L12,L13,L16,L20,L22,L23,L2 |
| 273000150001 | FERRITE CHIP;220OHM/100MHZ,2012, | L1 |
| 273000150013 | FERRITE CHIP;120OHM/100MHZ,2012, | PL1,PL2,PL501,PL502,PL503,PL |
| 273000150313 | CHOKE COIL;90OHM/100MHZ,20%,2012 | L14,L15,L18,L19,L517,L519 |
| 273000150332 | FERRIET CHIP;120OHM/100MHZ,2012, | L1,L11,L17,L21,L30,L506,L510,L |
| 273000500115 | CHOKE COIL;400uH MIN,120mΩ MAX; | L515 |
| 273000500150 | CHOKE COIL;4.7UH,+/-20%,5.7A,4.5 | PL510 |
| 273000500160 | CHOKE COIL;10UH,+/-30%,3A,2.8mm, | PL507 |
| 273000500164 | CHOKE COIL;0.56UH,+/-20%,25A,4mm | PL508,PL509 |
| 273000500168 | CHOKE COIL;4.7UH,+/-30%,8.7A,3.5 | PL505,PL506 |
| 273000610013 | FERRITE ARRAY;120OHM100MHZ,3216, | FA1,FA502 |
| 273001050039 | XSFORMER;10/100 BASE,LF-H80P,SMT | U512 |
| 273001050126 | XFMR;CI8.5,25T/2150T,292mH,Varni | T1 |
| 274011431449 | XTAL;14.318MHZ,32PF,50PPM,8*4.5, | X503 |
| 274012457430 | XTAL;24.576MHZ,16PF,50PPM,8*4.5, | X505 |
| 274012500420 | XTAL;25MHz,30PPM,16PF,8*4.5,2P,S | X504 |
| 274013276103 | XTAL;32.768KHZ,20PPM,12.5PF,CM20 | X502 |
| 274018000303 | XTAL;8MHZ,30PPM,16PF,8*4.5,2P,SM | X501 |
| 281101015001 | IC;MP1015EM-Z,CCFL CTRL,TSSOP20, | U1 |

| Part Number | Description | Location(S) |
|---|---|---|
| 281307085001 | IC;NC7SZ08P5,2-INPUT & GATE,SC70 | U11,U12,U508 |
| 282574108002 | IC;74AHC1G08,SINGLE AND GATE,SOT | U510 |
| 282574186002 | IC;74AHCT1G86,SINGLE,XOR,SOT23,S | U520 |
| 283467540001 | IC;EEPROM,M24C02-WMN6T,2K,SO8,SM | U2 |
| 283467540002 | IC;EEPROM,M93C46-WMN6T,64*16 BIT | U509 |
| 283468140003 | IC;FLASH,512K*8,PLCC32,LPC,Pm49F | |
| 283468180001 | IC;FLASH,512K*8,LPC & FWH,SST49L | |
| 284500086001 | IC;LM86,TEMPERATURE MTR,SO8 | U9 |
| 284500655003 | IC;ALC655,AUDIO CODEC,LQFP,48P,S | U519 |
| 284501623001 | IC;VT1623M,TV ENCODER,TQFP,64P,S | U2 |
| 284501634001 | IC;VT1634,LVDS TRANSMITTER,TQFP, | U501 |
| 284506103008 | IC;VT6103L,LAN-PHY,LQFP48,SMT | U515 |
| 284508235008 | IC;VT8235CE,SOUTH BRIDGE,BGA,487 | U511 |
| 284508800006 | IC;VIA K8N800CE,N.B.,BGA578,SMT | U502 |
| 284583950002 | IC;W83L950D-Ver.C,LPC_KBC,LQFP,8 | |
| 284595040001 | IC;ICS950405,SYSTEM CLK FOR AMD | U514 |
| 286002040001 | IC;BQ2040,GAS GAUGE,SO,16P,SMT | U3 |
| 286100212001 | IC;TPA0212,AMPLIFIER,TSSOP,24P,S | U521 |
| 286100358016 | IC;AZ358,DUAL OP AMP,SO8,SMT | U503 |
| 286100393004 | IC;LMV393,DUAL COMPARTOR,SSOP,8P | PU9 |
| 286300055001 | IC;TC55,3.3V,250mA,REG.,SOT89 | PU502 |
| 286300431014 | IC;SC431LCSK-.5,.5%,ADJ REG,SOT2 | PQ506 |
| 286300812002 | IC;S-812C,DECECTOR,SOT-89,PRC | U1 |
| 286300865001 | IC;G965,LDO,SO8,SMT | PU11 |
| 286301410002 | IC;CB1410Q_B0,PCI/CARDBUS,LQFP,1 | U10 |

# 9. Spare Parts List (7)

| Part Number | Description | Location(S) |
|---|---|---|
| 286301414001 | IC;MM1414,PROTECTION,TSOP-20A,PR | U5 |
| 286301470001 | IC;SC1470,PWM CTRL,TSSOP,14P,SMT | PU18 |
| 286301772001 | IC;MAX1772,PWM,QSOP,28P | PU8 |
| 286302211006 | IC;CP2211,POWER DISTRI SW,REV.C1 | |
| 286302211008 | IC;CP2211,POWER DISTRI SW,REV D3 | U517 |
| 286302951015 | IC;LP2951ACM,VOLTAGE REGULATOR,S | PU6 |
| 286302996001 | IC;G2996,DDR,GMT,SOP8FD,SMT | PU19 |
| 286303728002 | IC;LTC3728LX,PWM CTRL,LTC,5X5 QF | PU4 |
| 286306207001 | IC;ISL6207CB,PWM DRIVER,SO8,SMT | PU14,PU15 |
| 286306559005 | IC;ISL6559CR,MULTI-PHASE PWM CTL | PU13 |
| 286308804002 | IC;AME8804AEEY,ADJ,0.3A,LDO,SOT2 | PU12 |
| 286308824002 | IC;AME8824,0.3A,LDO REG.,SOT26 | PU10 |
| 286309702001 | IC;RT9702A,POWER DISTRI SW,1.1A, | U4,U504,U506,U7 |
| 286369229301 | IC;G692L293T,RESET CIRCUIT,2.93V | U505 |
| 288100014010 | DIODE;SS14,40V,1A,SMA,VISHAY | PD11 |
| 288100018003 | DIODE;UDZS18B,ZENER,18V,SOD-323, | ZD3,ZD4 |
| 288100032013 | DIODE;BAS32L,VRRM75V,MELF,SOD-80 | PD508 |
| 288100034004 | DIODE;SSA34,40V,3A,SMA | PD6,PD7 |
| 288100054002 | DIODE;BAT54C,SCHOTTKY DIODE,SOT2 | D16,D504 |
| 288100056005 | DIODE;UDZ5.6B,ZENER,5.6V,UMD2,SM | ZD1,ZD2,ZD5 |
| 288100099012 | DIODE;BAV99LT1,70V,450MA,SOT-23, | PD505,PD506 |
| 288100140008 | DIODE;SCS140P,40V,1A,SECOS,SMT | PD8,PD9 |
| 288100340008 | DIODE;B340LA,40V,3A,SMA,DIODES,S | PD3 |
| 288100541002 | DIODE;BAT54ALT1,COM. ANODE,SOT-2 | D508,PD2,PD507 |
| 288100701002 | DIODE;BAV70LT1,70V,225MW,SOT-23 | D4,PD502,PD503 |

| Part Number | Description | Location(S) |
|---|---|---|
| 288101040006 | DIODE;SBM1040,10A,SCHOTTKY,POWER | PD13,PD504 |
| 288104148001 | DIODE;RLS4148,200MA,500MW,MELF,S | D5 |
| 288105524002 | DIODE;BZV55-C2V4,ZENER,5%,SOD-80 | PD10,PD5 |
| 288105524003 | DIODE;BZV55-C24,ZENER,5%,SOD-80, | PD501 |
| 288105533001 | DIODE;BZV55-C3V3,ZENER,5%,SOD-80 | PD12 |
| 288105556001 | DIODE;BZV55-C5V6,ZENER,5%,SOD-80 | PD1,PD4 |
| 288114148004 | DIODE;1N4148WS,75V,200mW,SOD-323 | D1 |
| 288200144019 | TRANS;DTC144WK,NPN,SOT-23,SMT,PA | PQ10,PQ11,PQ18,PQ19,PQ8,Q12 |
| 288200144020 | TRANS;DTC144TKA,NPN,SOT-23,SMT,P | Q11,Q13,Q19,Q2,Q20,Q503,Q510 |
| 288200144023 | TRANS;DTA144WK,PNP,SOT23,SMT,PAN | PQ12 |
| 288200301001 | TRANS;FDV301N,N-CHANNEL,SOT23 | Q501,Q502 |
| 288203400001 | TRANS;AO3400,N-MOSFET,SOT-23 | Q1 |
| 288203401001 | TRANS;AO3401,P-MOSFET,SOT-23 | PQ17 |
| 288203409001 | TRANS;AO3409,P-MOSFET,SOT-23 | Q504 |
| 288203707002 | TRANS;IRFR3707Z,N-MOSFET,56A,30V | PQ508,PQ509 |
| 288203709002 | TRANS;IRFR3709Z,N-MOSFET,86A,30V | PQ507,PQ510 |
| 288203906018 | TRANS;MMBT3906L,PNP,Tr35NS,TO236 | PQ16 |
| 288204350001 | TRANS;PBSS4350Z,50V,5A,SOT223 | PQ13 |
| 288204406001 | TRANS;AO4406,N-MOS,.0165OHM,SO8 | PU16 |
| 288204407001 | TRANS;AO4407,P-MOS,.01OHM,SO8,SM | PQ502,PQ7 |
| 288204409001 | TRANS;AO4409,P-MOSFET,SO-8P,MSL, | Q2A,Q2B,Q3B,Q3C |
| 288204422001 | TRANS;AO4422,24mOHM,N-MOSFET,SOI | PQ504,PU17 |
| 288204788001 | TRANS;SI4788CY,P-MOS,5A1.8~5.5V, | PU1,PU2,PU3,PU5,PU503,PU504 |
| 288204832001 | TRANS;SI4832DY,N-MOSFET,.028OHM, | PQ505 |
| 288204912001 | TRANS;AO4912,24mOHM ,SMT | PQ503,PU501 |

# 9. Spare Parts List (8)

| Part Number | Description | Location(S) |
|---|---|---|
| 288208107001 | TRANS;TPC8107,13A/30V,P-MOSFET,S | |
| 288227002001 | TRANS;2N7002LT1,N-CHANNEL FET,SO | PQ1,PQ14,PQ15,PQ2,PQ3,PQ4,P |
| 291000000203 | CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM | J2 |
| 291000001206 | CON;MINI PCI SOCKET,P124,QTC,C10 | J503 |
| 291000010303 | CON;HDR,MA,3P*1,1.25MM,H4.2,ST,S | J505 |
| 291000011101 | CON;HDR,MA,11P*1,1.25,ST,SMT | J2 |
| 291000012022 | CON;HDR,MA,10P*2,1MM,H4.25,ST,SM | J1 |
| 291000020204 | CON;HDR,MA,2P*1,3.5MM,R/A,SMT,SM | |
| 291000020206 | CON;HDR,MA,2P*1,1.25MM,H2.57,R/A | J4,J507,J513,J515 |
| 291000020221 | CON;HDR,MA,11P*1,1.25MM,R/A,ACES | |
| 291000021104 | CON;HDR,MA,11P*1,1.25,R/A,3811Y- | CN1 |
| 291000023008 | CON;HDR,FM,15P*2,0.8MM.H5,R/A,SM | J514 |
| 291000024421 | CON;HDR,MA,22P*2,R/A,SUYIN,20038 | J512 |
| 291000025028 | CON;HDR,FM,25P*2,R/A,SUYIN,80094 | J508 |
| 291000151214 | CON;FPC/FFC,12P,0.5MM,H2MM,R/A,T | J9 |
| 291000152603 | CON;FPC/FFC,26P,1MM,R/A,KBD,SMT | J8 |
| 291000256843 | CON;IC CARD,68P,UP,STANDOFF 0.0 | J10 |
| 291000612003 | DIMM SOCKET;DDR,200P,0.6MM,H9.2, | J510 |
| 291000612028 | DIMM SOCKET;DDR,200P,0.6MM,H9.2, | |
| 291000617542 | IC SOCKET;AMD K8 BGA-PGA754-SKT, | U507 |
| 291000810607 | CON;PHONE JACK,6P,SG-2SJ-S820 | J11,J12 |
| 291000811008 | CON;PHONE JACK,2 IN 1,7.0MM,ALLT | J509 |
| 294011200016 | LED;GREEN,H0.8,0603,CL-190G,SMT | D11,D12,D13,D14,D15 |
| 294011200043 | LED;RE/GR,H0.8,L1.9,W1.6,19-22SR | LED1 |
| 294011200043 | LED;RE/GR,H0.8,L1.9,W1.6,19-22SR | LED2 |

| Part Number | Description | Location(S) |
|---|---|---|
| 294011200069 | LED;GREEN,19-21VGC/TR8,LED_CL190 | LED3,LED5 |
| 294011200069 | LED;GREEN,19-21VGC/TR8,LED_CL190 | LED4,LED6 |
| 295000010009 | FUSE;NORMAL,5A/32VDC,3216,SMT | PF502,PF503,PF504,PF505 |
| 295000010016 | FUSE;NORMAL,6.5A/32VDC,3216,SMT | PF501 |
| 295000010044 | FUSE;1.1A/6V,POLY SWITCH,1210,SM | F2 |
| 295000010057 | FUSE;228R,139C',5A/250V,SMT,PRC | TF1 |
| 295000010116 | FUSE;FAST, 10A, 86VDC, 6125,SMT | PF1 |
| 295000010120 | FUSE;FAST,1.5A,63V,1206,SMT,PRC | F1 |
| 295000010149 | FUSE;FAST,1.5A,63VDC,1206,SMT,04 | |
| 297004010001 | SW;PUSH BUTTOM,5P,SPST,12VDC,50m | SW2,SW3,SW4 |
| 297140200002 | SW;COVER SWITCH,SPST,.1A,30V,4P, | SW1 |
| 310111103011 | THERMISTOR;10K,1%,RA,DISK,103AT- | T1 |
| 312078206331 | EC;820U ,2.5V,+-20%, 8*8mm, PSC2 | PC537,PC538,PC541,PC542 |
| 316677000002 | PCB;PWA-LYNX/BATTERY BD,PWR | |
| 316682200001 | PCB;PWA-INVERTER BD (DA-1A08-B); | R0E |
| 316685200002 | PCB;PWA-8889/M BD | R03 |
| 322677000003 | CABLE;FFC,T/P,LYNX | |
| 323768550002 | DDR SODIMM MODULE;256MB,PC2700,7 | |
| 324180786964 | IC;CPU,AMD Mobile K8 Dublin 2800 | |
| 331000000314 | CON HOLDER;PCMCIA,R-BTN ,MPT,929 | J10 |
| 331000007005 | CON;BATTERY,7P,2.5MM,H9,R/A,DIP, | PJ502 |
| 331000007019 | CON;BATTERY,7P,2.5MM,25032A-07G1 | |
| 331000008089 | CON;USB,FM,H15.64,R/A,4P*2,SUYIN | J504,J506 |
| 331660020004 | DIMM SOCKET;DDR SODIMM 200P, CA0 | J511 |
| 331720015006 | CON;D,FM,15P,2.29,R/A,3ROW | J502 |

# 9. Spare Parts List (9)

| Part Number | Description | Location(S) |
|---|---|---|
| 331870004021 | CON;MINI DIN,4P,R/A,SUYIN,35144A | J501 |
| 331910002006 | CON;POWER JACK,2P,20VDC,5A,DIP | PJ501 |
| 332110020042 | WIRE;#20,UL1007,70MM,RED,PRC | |
| 332110020067 | WIRE;#20,UL1007,40MM,BLACK,PRC | |
| 332110020089 | WIRE;#20,UL1007,L105mm,RED,PRC | |
| 332110020096 | WIRE;#20,UL1007,40MM,BLACK,YIYI; | |
| 332110020104 | WIRE;#20,UL1007,105MM,RED,YIYI;P | |
| 332110020108 | WIRE;#20,UL1007,70MM,RED,YIYI;PW | |
| 332110026007 | WIRE;#26,UL1007,80MM,YELLOW | |
| 332110026124 | WIRE;#26,UL1007,80MM,YELLOW,YIYI | |
| 332110026134 | WIRE;#26,UL1007,135MM,BLACK,PRC, | |
| 332110026135 | WIRE;#26,UL1007,40MM,ORANGE,PRC, | |
| 332810000033 | PWR CORD;125V/7A,2P,BLACK,AMERIC | |
| 333020000003 | SHRINK TUBE;600V,105'C,D0.8*5MM, | |
| 333050000107 | SHRINK TUBE;UL,600V,105'C,ID2.5* | |
| 333678700002 | SHRINK TUBE; 600V, 125℃, Φ2L8m | |
| 335152000062 | FUSE;LR4-730,POLY SWITCH,PRC | |
| 335152000100 | FUSE; THERMAL,SF91E-1/94℃,10A/2 | |
| 338536010006 | BATTERY;LI,3.6V/2.0AH,18650,PANA | |
| 339115000046 | MICROPHONE;-62dB+-2dB,D6.0*H2.7, | MIC1 |
| 340677000001 | SPEAKER ASSY;L,LYNX | |
| 340677000009 | SHIELDING ASSY;HDD,LYNX | |
| 340677000013 | SPEAKER ASSY;R,LYNX | |
| 340677000098 | COVER;ASSY,HDD,H-R,LYNX | |
| 340677000103 | SPEAKER ASSY;8OHM,1W,35.0*16.0*4 | |

| Part Number | Description | Location(S) |
|---|---|---|
| 340677000104 | SPEAKER ASSY;8OHM,1W,35.0*16.0*4 | |
| 340682810003 | COVER ASSY;LCD,8089P | |
| 340682810012 | BEZEL ASSY;LITEON,852S,ID2,8089P | |
| 340685200001 | SHIELDING ;ASSY,COVER,8889 | |
| 340685200003 | COVER;ASSY,DOOR,8889 | |
| 340685200004 | HOUSING;ASSY,8889 | |
| 340685200006 | HEATSINK;ASSY,ALRO,8889 | |
| 340685200008 | COVER;ASSY,ID2,8889 | |
| 340685200009 | HOUSING ASSY;LCD,ID2,8889 | |
| 340685200010 | COVER ASSY;KB,ID2,8889 | |
| 341677000002 | SPRING;SCREW,HEATSINK,LYNX | |
| 342503200003 | CONTACT PLATE;W4L18T0.15,7521/GR | |
| 342503400004 | CONTACT PLATE;W5L45T0.13,7170LI, | |
| 342503400006 | CONTACT PLATE;W5L45T0.13,7170LI, | |
| 342503400007 | CONTACT PLATE;W5L45T0.13 ,1/3T,7 | |
| 342665500010 | CFM-SUYIN,S-STANDOFF,#4-40H4.8,N | |
| 342672200010 | BRACKET;CD-ROM,8500 | |
| 342673100025 | CONTACT PLATE;W5L46T0.13 ,2T,806 | |
| 342677000001 | HINGE;LCD L,LYNX | |
| 342677000002 | HINGE;LCD R,LYNX | |
| 342677000012 | BRACKET;LCD 15"HANNSTAR,L,LYNX | |
| 342677000013 | BRACKET;LCD 15"HANNSTAR,R,LYNX | |
| 342677000014 | SMT NUT;A40M20-50,EMI STOP,LYNX | MTG2,MTG3 |
| 342677000019 | CONTACT PLATE;W5L76T0.13 ,1/3T,L | |
| 342677000020 | HINGE;LCDL,LYNX,SZS (CHINA) | |

# 9. Spare Parts List (10)

| Part Number | Description | Location(S) |
|---|---|---|
| 342677000021 | HINGE;LCDR,LYNX,SZS (CHINA) | |
| 342677000028 | HINGE;LCD L,LYNX-AMD(BANIAS),15" | |
| 342677000029 | HINGE;LCD R,LYNX-AMD(BANIAS),15" | |
| 342685200003 | FINGER;EMI GROUNDING SMD FINGER | TP39,TP43 |
| 343674300005 | HEATSINK;NORTH BRIDGE,E-NOTE | |
| 343685200001 | EMI FINGER;3X2MM,H2.5,SME-0025RA | TP44,TP45 |
| 343685200004 | EMI FINGER;3X2MM,H3,MSME-0030RA, | TP13,TP14,TP15,TP16,TP36,TP |
| 343685200005 | EMI FINGER;2X2MM,H5.5,MSML-0055A | TP505 |
| 344677000022 | COVER;BATTERY,LYNX | |
| 344677000138 | COVER;HINGE,H-R,LYNX | |
| 344677000140 | HOUSING;BATT,H-R,LYNX | |
| 344682810004 | BUTTON;T/P,8089P | |
| 345677000006 | GASKET;AUDIO,LYNX | |
| 345677000007 | GASKET;DC_JACK,LYNX | |
| 345677000008 | GASKET;TV_OUT,LYNX | |
| 345677000010 | GASKET;RJ_COMBO,LYNX | |
| 345677000024 | CONDUCTIVE TAPE;INSULATOR MB,LYN | |
| 345682600003 | SPONGE;HOUSING,LCD,8389 | |
| 346503100005 | INSULATOR;5,BATTERY ASSY,7521Li | |
| 346503200202 | INSULATOR;BATT ASSY,ONE ROUND,BL | |
| 346503400503 | INSULATOR;BATT ASSY,W7L13,8175 | |
| 346669900004 | INSULATOR;INVERTER,7170 | |
| 346670500014 | INSULATOR;MDC,TETRA | |
| 346677000009 | INSULATOR;FOR 3CELL DOUBLE-FA,LY | |
| 346677000012 | MYLAR;COVER,LCD,LYNX | |

| Part Number | Description | Location(S) |
|---|---|---|
| 346677000028 | INSULATOR;SINGLE-FA,FOR PCB-A,LY | |
| 346677000029 | INSULATOR;SINGLE-FA,FOR PCB-B,LY | |
| 346677000030 | INSULATOR;BATT ASSY,POLY,W30L64, | |
| 346677000031 | INSULATOR;FOR 3 CELLS,SINGLE-FA, | |
| 346677000032 | INSULATOR;BATT ASSY,THERMAL FUSE | |
| 346677000037 | INSULATOR;SPEAKER,LYNX | |
| 346677000042 | AL FOIL;LCD,BANIAS,LYNX | |
| 346677000044 | INSULATOR;W8L45T0.8, DOUBLE-FA,L | |
| 346682600005 | INSULATOR;T/P-BUTTON,8689 | |
| 346685200002 | INSUATOR;MB,8889 | |
| 346685200003 | INSUATOR;HEATSINK,8889 | |
| 346685200004 | INSUATOR;NORTHBRIDGE,8889 | |
| 346685200008 | INSULATOR;PCMCIA,8889 | |
| 346685200009 | INSULATOR;DDR,8889 | |
| 346867700001 | FILM;PROTECT FOR APOLLON BATTERY | |
| 347108020015 | GASKET;1,08,020,015 | |
| 347110005030 | GASKET;1,10,005,030 | |
| 361200003047 | SOLDER PASTE;NO CLEAN,RMA,CK3000 | |
| 361400003003 | JET-MELT ADHESIVES;3478-Q,5/8in* | |
| 361400003005 | ADHESIVE;HEAT,TRANSFER,HTA-48(W) | |
| 361400003030 | ADHESIVE;ABS+PC PACK,G485,CEMIDA | |
| 365350000003 | SOLDER WIRE;0.8MM,SN43/PB43/BI14 | |
| 370102010204 | SPC-SCREW;M2L2,NIW/NLK,K-HD | |
| 370102010257 | SPC-SCREW;M2L2.5,K-HD(t0.5),NIW | |
| 370102010404 | SPC-SCREW;M2L4,K-HD,NIB | |

# 9. Spare Parts List (11)

| Part Number | Description | Location(S) |
|---|---|---|
| 370102010502 | SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NL | |
| 370102010502 | SPC-SCREW;M2 L5,NIB,K-HD,t0.8,NL | |
| 370102030301 | SPC-SCREW;M2L3,K-HD,1,NIB/NLK | |
| 370102030301 | SPC-SCREW;M2L3,K-HD,1,NIB/NLK | |
| 370102610304 | SPC-SCREW;M2.6L3,KHD,D4.4,t0.45, | |
| 370102610405 | SPC-SCREW;M2.6L4,NIW,K-HD,t=0.8, | |
| 370102610501 | SPC-SCREW;M2.6L5,NIW,K-HD,NYLOK | |
| 370102610602 | SPC-SCREW;M2.6 L6,NIB,K-HD,t0.8, | |
| 370102610603 | SPC-SCREW;M2.6L6,K-HD,NIB/NLK | |
| 370102610603 | SPC-SCREW;M2.6L6,K-HD,NIB/NLK | |
| 370103010405 | SPC-SCREW;M3L4,NIW,K-HD,T0.3 | |
| 371102010252 | SCREW;M2L2.5,K-HEAD(+),NIB/NLK | |
| 371102010252 | SCREW;M2L2.5,K-HEAD(+),NIB/NLK | |
| 371102030305 | SCREW;M2L3,K-HEAD(+),NIB | |
| 371102610406 | SCREW;M2.6L4,K-HEAD(+),NIB | |
| 411682200001 | PWA;PWA-INVERTER BD,DA-1A08-B,PW | |
| 411682200002 | PWA;PWA-INVERTER BD,SMT,DA-1A08- | |
| 411682200003 | PWA;PWA-INVERTER BD,SMT TOP,DA-1 | |
| 411682200004 | PWA;PWA-INVERTER BD,SMT BOT,DA-1 | |
| 411685200017 | PWA;PWA-8889,MOTHER BD | |
| 411685200018 | PWA;PWA-8889,MOTHER BD,T/U | |
| 411685200019 | PWA;PWA-8889,MOTHER BD,SMT | |
| 411685200024 | PWA;PWA-8889/BATT PANASONIC,9CEL | |
| 411685200025 | PWA;PWA-8889/BATT PANASONIC,9CEL | |
| 412678800001 | PCB ASSY;FAX MODEM 56K,1456VQL4A | |

| Part Number | Description | Location(S) |
|---|---|---|
| 412682200001 | PCB ASSY;INVERTER BD,DA-1A08-B,P | |
| 413000020433 | LCD;LTN150XB- L03,15",XGA,SAMSUN | |
| 416268521001 | LT PF;SAMSUNG,XGA,LTN150XB-L03,I | |
| 422677000005 | WIRE ASSY;INVERTER,LYNX | |
| 422677000008 | WIRE ASSY;BATT TO MB,FOR LYNX,MO | J513 |
| 422677000010 | WIRE ASSY;INVERTER,LYNX,HIGH-TEK | |
| 422677000017 | WIRE ASSY;LCD 15",SAMSUNG,LYNX | |
| 422685200002 | WIRE ASSY;MDC,8889 | |
| 422685200004 | WIRE ASSY;ANTENNA,JEM,8889 | |
| 431685210001 | CASE KIT;ID2,8889 | |
| 441685200024 | BATT ASSY;LI,9-CELL,2000mAH,8889 | |
| 441685200029 | BATT ASSY;8889/11.1V,6AH,PANASON | |
| 441685210001 | LCD ASSY;SAMSUNG,XGA,LTN150XB-L0 | |
| 442164900021 | TOUCHPAD MODULE;TM41PUC2311-2,DI | |
| 442681400051 | AC ADPT ASSY;19V,3.43A,HIPRO HP | |
| 451685200004 | HDD ME KIT;8889 | |
| 451685200005 | ROM ME KIT;8889 | |
| 451685200007 | LABEK KIT;N-B,8889 | |
| 451685210001 | LCD ME KIT;SAMSUNG,XGA,LTN150XB- | |
| 451685210003 | HOUSING KIT;ID2 ;8889 | |
| 461685200003 | PACKING KIT;N-B,8889 | |
| 461685200006 | PACKING KIT;8889/11.1V,6AH,PANAS | |
| 481685200001 | F/W ASSY;SYS/VGA BIOS,8889 | U516 |
| 481685200002 | F/W ASSY;KBD CTRL,8889 | U6 |
| 523402379051 | HDD DRIVE;40GB,2.5",MHT2040AT,V4 | |

# 9. Spare Parts List (12)

| Part Number | Description | Location(S) |
|---|---|---|
| 523468520004 | HDD ASSY;40G,FUJITSU,MHT2040AT,V | |
| 523468520008 | DVD DUAL ASSY;LITE-ON,SOSW-852S, | |
| 523482389023 | DVD±RW Dual (DVD-Rx8) Drive;SOS | |
| 526268521001 | LTXXNON;8889/T5AC/0C04H/1XUSTW/3 | |
| 531020237826 | KBD;88,US,K011718M4,8089P | |
| 541668520001 | AK;BOX ,8889 DVT | |
| 600100010009 | SOLDER WIRE;63/37,0.8,CM,N/C,PRC | |
| 600100010009 | SOLDER WIRE;63/37,0.8,CM,N/C,PRC | |
| 622200000008 | TAPE;CARTON,2.5"W,30M/RL,PRC | |
| 624200010140 | LABEL;5*20,BLANK,COMMON | |
| 624200010140 | LABEL;5*20,BLANK,COMMON | |
| 624200010140 | LABEL;5*20,BLANK,COMMON | |
| 624200010140 | LABEL;5*20,BLANK,COMMON | |
| 627207522141 | CAP;220P ,50V ,10%,0603,X7R,SMT | C25 |
| 628820014401 | TRANS;DTA144EKA,PNP,100MA,50V,SO | Q6,Q7 |
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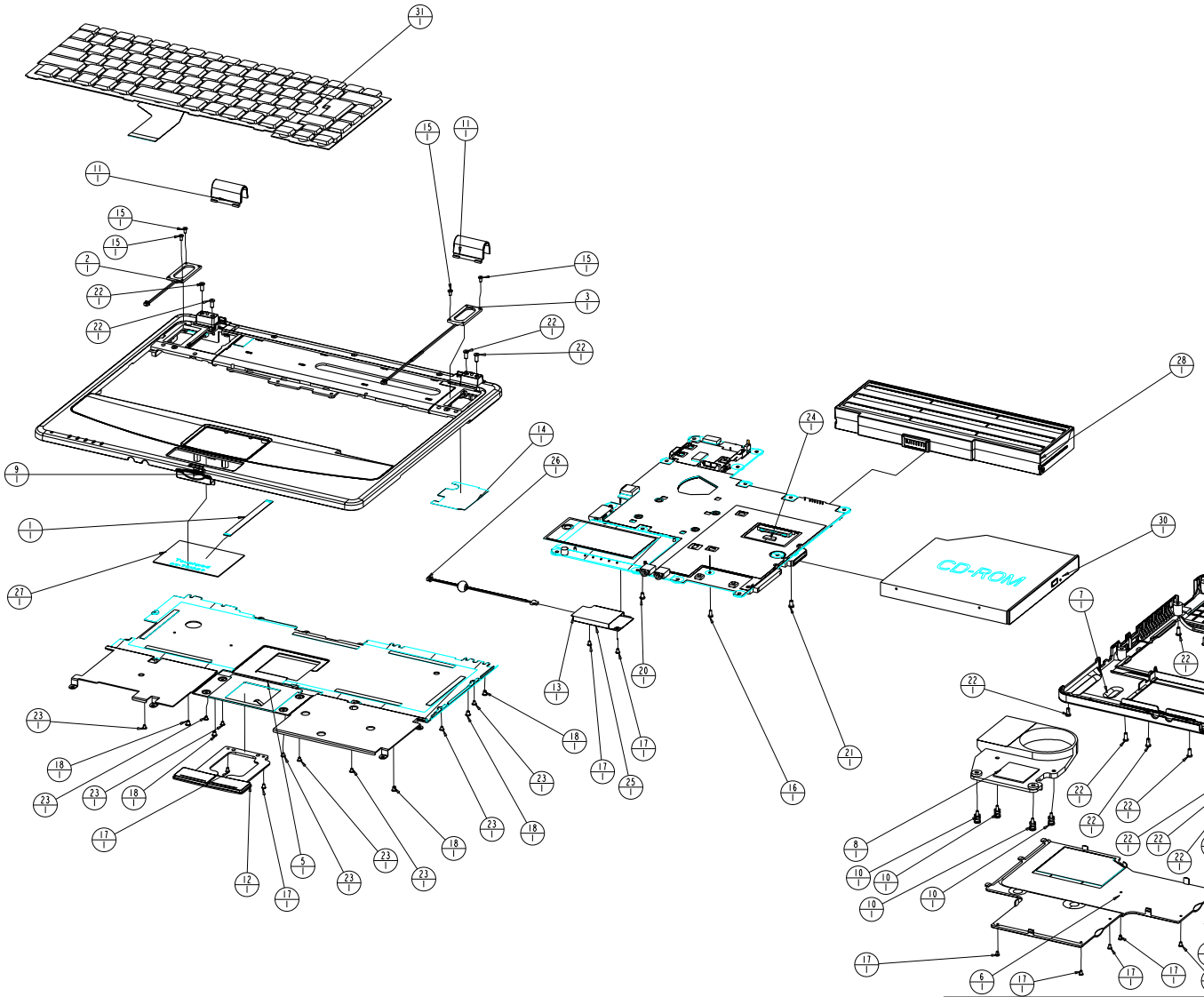
| | | **P/N:526268521001** |



| ITEM | PART NO | PART NAME | Q'TY | TYPE |
|---|---|---|---|---|
| 1 | 322677000003 | CABLE;FFC,T/P,LYNX | 1 | PART |
| 2 | 340677000001 | SPEAKER ASSY;L,LYNX | 1 | ASSEMBLY |
| 3 | 340677000013 | SPEAKER ASSY;R,LYNX | 1 | ASSEMBLY |
| 4 | 340677000098 | COVER ASSY;HDD,H-R,LYNX | 1 | ASSEMBLY |
| 5 | 340685200001 | SHIELDING ASSY;COVER,8889 | 1 | ASSEMBLY |
| 6 | 340685200003 | COVER ASSY;DOOR,8889 | 1 | ASSEMBLY |
| 7 | 340685200004 | HOUSING;ASSY,8889 | 1 | ASSEMBLY |
| 8 | 340685200006 | HEATSINK ASSY;8889 | 1 | ASSEMBLY |
| 9 | 340685200008 | COVER;ASSY,ID2,8889 | 1 | ASSEMBLY |
| 10 | 341677000002 | SPRING-SCREW-HEATSINK-LYNX | 4 | PART |
| 11 | 344677000138 | COVER;HINGE,H-R,LYNX | 2 | PART |
| 12 | 344682810004 | BUTTON;T/P,8089P | 1 | PART |
| 13 | 346670500014 | INSULATOR;MDC,TETRA | 1 | PART |
| 14 | 346677000037 | INSULATOR;SPEAKER,LYNX | 1 | PART |
| 15 | 370102010407 | SPC-SCREW;M2L4,K-HD,NIB/NLK | 4 | PART |
| 16 | 370102010502 | SPC-SCREW;M2L5,NIB,K-HD,t0.8,NLK | 1 | PART |
| 17 | 370102030301 | SPC-SCREW; M2L3,K-HEAD,I,NIB,NLK | 12 | PART |
| 18 | 370102610303 | SPC-SCREW;M2.6L3,KHD,D4.4t0.45,N | 5 | PART |
| 19 | 370102610401 | SPC-SCREW;M2.6L4,K-HD,t0.8,NIB/N | 3 | PART |
| 20 | 370102610405 | SPC-SCREW; M2.6L4 K-HEAD,NIW | 1 | PART |
| 21 | 370102610501 | SPC-SCREW;M2.6L5,NIW,K-HD,NYLOK | 1 | PART |
| 22 | 370102610603 | SPC-SCREW; M2.6L6 K-HEAD,NIB/NLK | 23 | PART |
| 23 | 371102010252 | SCREW;M2L2.5,K-HEAD(+),NIB/NLK | 12 | PART |
| 24 | 411685200017 | PWA;PWA-8889,MOTHER BD | 1 | ASSEMBLY |
| 25 | 412671800001 | PCB ASSY;FAXMODEM,56K,MDC,GP2 | 1 | PART |
| 26 | 422685200002 | WIRE ASSY;MDC,8889 | 1 | ASSEMBLY |
| 27 | 442110500009 | TOUCH PAD MODULE;90425 | 1 | PART |
| 28 | 442677000013 | BATT ASSY;11.1V/6.0AH,LI,PAN | 1 | ASSEMBLY |
| 29 | 451677000091 | HDD ME KIT;LYNX-AMD | 1 | ASSEMBLY |
| 30 | 523468520002 | ODD-MEKIT-QSI-041-8889 | 1 | ASSEMBLY |
| 31 | 531020237661 | KBD;89,US,K011718M1,LYNX | 1 | PART |

| ITEM | CONTENTS OF CHANGE | RVS | CHK | APV | M/D/Y |
|---|---|---|---|---|---|
| | | | | | / / |
| | | | | | / / |
| | | | | | / / |
| | | | | | / / |
| | | | | | / / |

| TOL ± RANGE | M1 | M2 | S1 | S2 | P1 | P2 | C | B |
|---|---|---|---|---|---|---|---|---|
| 0-6 | .05 | 0.1 | .15 | 0.2 | .05 | 0.1 | 0.5 | .15 |
| 6-30 | 0.1 | 0.2 | .15 | .25 | 0.1 | .15 | 1 | .15 |
| 30-80 | .15 | .25 | 0.2 | 0.3 | 0.2 | 0.4 | 2 | .25 |
| 80-180 | .15 | 0.3 | .25 | .45 | 0.4 | 0.8 | 3 | .25 |
| 180-315 | 0.2 | 0.5 | 0.4 | 0.6 | 0.6 | 1.2 | 3 | 0.3 |
| 315-800 | 0.3 | 0.8 | 0.7 | 1.1 | 0.8 | 1.5 | 4 | 0.5 |

| | | | | | |
|---|---|---|---|---|---|
| DATE | 06-May-04 | MATERIAL | SEE NOTES | TREATMENT | REMARK |
| UNIT | MM | SCALE | 0.50 | DRAWING NAME | HOUSING-KIT-ID2-8889 |
| DRAWN | DESIGNED | CHECKED | APPROVED | MATERIAL NO. | MF 451 6852 10003 A 00 |

MiTAC Technology Corp.

model name:STRU-SYSTEM-8689 | file name:8889-HOUSING-KIT | SHEET NO. 1 of 1

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# MODEL : 8889

# Revision 02

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| CPU-K8 (2/2) | 5 |
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| VIA K8N800 (2/2) | 7 |
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| DDR_SODIMM (2/2) | 9 |
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| DRAW | DESIGN | CHECK | ISSUED |
|---|---|---|---|
| | | | |

## POWER STATES

| STATE / SIGNAL | VOTAGE | POWER ON | STR (S3) | STD (S4) | MEC-OFF (S5) | REMARK |
|---|---|---|---|---|---|---|
| SUSB# | - | HIGH | LOW | LOW | LOW | |
| SUSC# | - | HIGH | HIGH | LOW | LOW | |
| ADP | +19V | O | O | O | O | |
| BATTERY | +12V | O | O | O | O | |
| +5VA | +5V | O | O | O | O | |
| +3VA | +3.3V | O | O | O | O | |
| +5VSB | +5V | O | O | O | X | |
| +3VSB | +3.3V | O | O | O | X | |
| +5V | +5V | O | O | X | X | |
| +3V | +3.3V | O | O | X | X | |
| +2.5V | +2.5V | O | O | X | X | |
| +1.25V | +1.25V | O | O | X | X | |
| +5VS | +5V | O | X | X | X | |
| +3VS | +3.3V | O | X | X | X | |
| +2.5VS | +2.5V | O | X | X | X | |
| +2.5VDDA | +2.5V | O | X | X | X | |
| +1.5VS | +1.5V | O | X | X | X | |
| +1.2VLDTA | +1.2V | O | X | X | X | |
| +CPU_CORE | +1.2V | O | X | X | X | |

## IDSEL

| IDSEL | CHIP |
|---|---|
| AD20 | CardBus |
| AD21 | MiniPCI |
| | |
| | |

## I2C / SMB Address

| DEVICE | WRITE ADDRESS | READ ADDRESS |
|---|---|---|
| CLK GEN | D2 | D3 |
| DIMM0 | A0 | A1 |
| DIMM1 | A2 | A3 |
| G781 | 98 | 99 |

## BUS MASTER

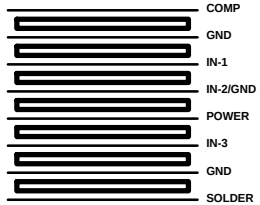
| REQ/GNT | CHIP |
|---|---|
| -REQ0/-GNT0 | CardBus |
| -REQ1/-GNT1 | |
| -REQ2/-GNT2 | MINI PCI |
| -REQ3/-GNT3 | |

## PCIINT

| PCIINT | CHIP |
|---|---|
| INTA# | VGA |
| INTB# | CardBus |
| INTC# | MiniPCI |
| INTD# | MiniPCI |
| INTE# | |

| | | |
|---|---|---|
| +3VA | VT8235<br>W83L950D | 5uA<br>20mA |
| +CPU_CORE | CPU | 30A |
| +5V | USB PORT * 4<br><br>MIMIPCI | 2A<br><br>300mA |
| +5VS | CP2211<br>CRT<br>HDD<br>ODD<br>MINIPCI<br>MDC<br>TPA0212<br>ALC655 | 1A<br>1A<br>1.5A<br>1.8A<br>100mA<br>500mA<br>1A<br>50mA |
| +3VSB | VT8235 | 160mA |
| +3V | CB1410<br><br>VT6103L<br>MIMIPCI | 200mA<br><br>130mA<br>380mA |
| +3VS | CP2211<br>K8N800<br>CLK_GEN<br>LCDVCC<br>VT8235<br>CB1410<br>ALC655<br>LPC BIOS ROM<br>VT6103L<br>MIMIPCI<br>W83L950D | 1A<br>400mA<br>360mA<br>1A<br>15mA<br>15mA<br>200mA<br>15mA<br>10mA<br>430mA<br>20mA |
| +2.5VSB | VT8235 | 6mA |
| +2.5V | CPU<br>DDR_DIMM | 3A<br>4A |
| +2.5VS | VT8235<br>VT1634 | 400mA<br>44mA |
| +1.5VS | K8N800 | 1A |
| +1.25V | DDR_DIMM | 1A |
| +1.2VLDT | K8N800<br>CPU | 200mA<br>500mA |

## Board Stackup-up



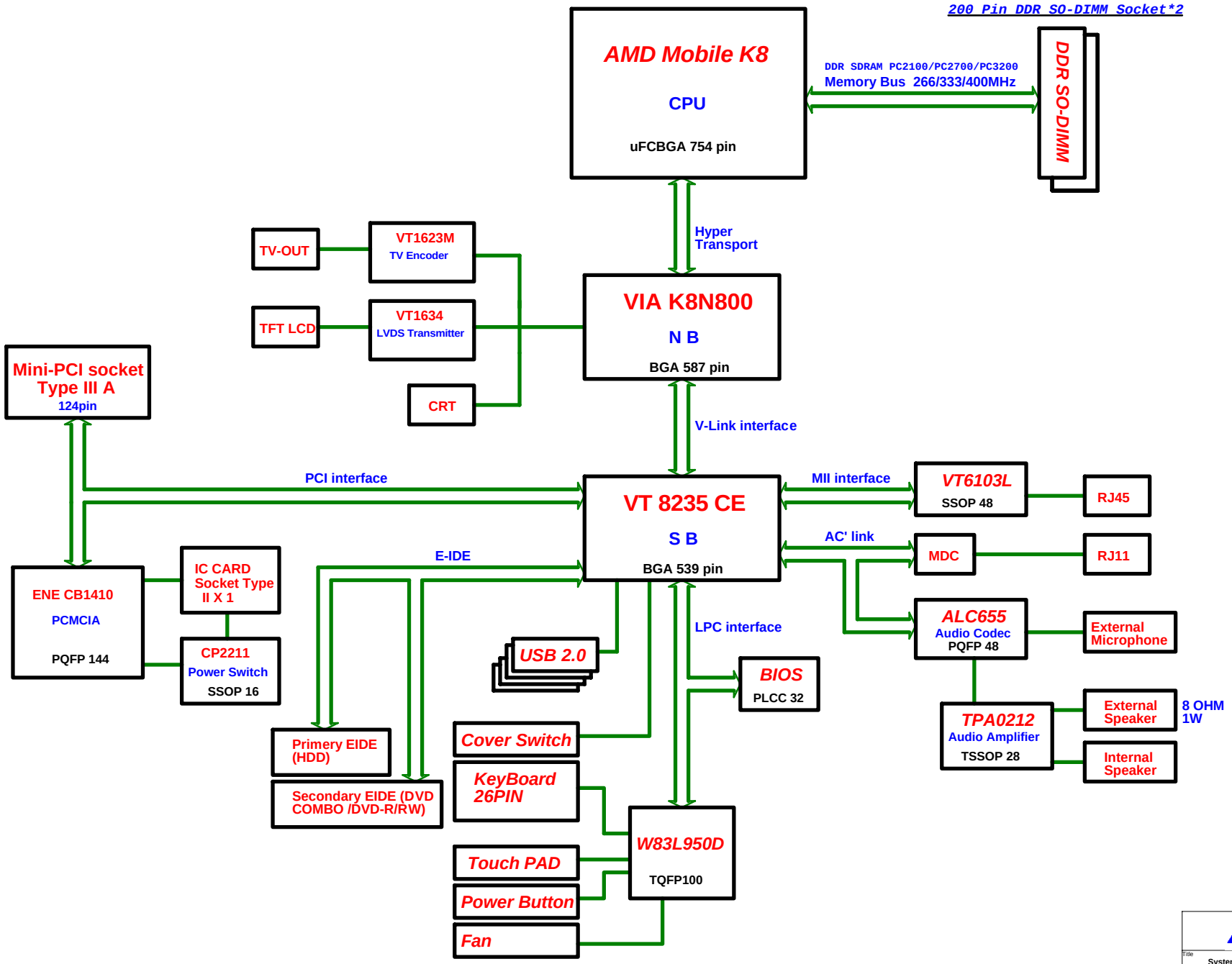

MiTAC

Title: COVER SHEET

Size | Document Number: 316685200002 | Rev: R02

Date: Monday, August 23, 2004 | Sheet 1 of 30

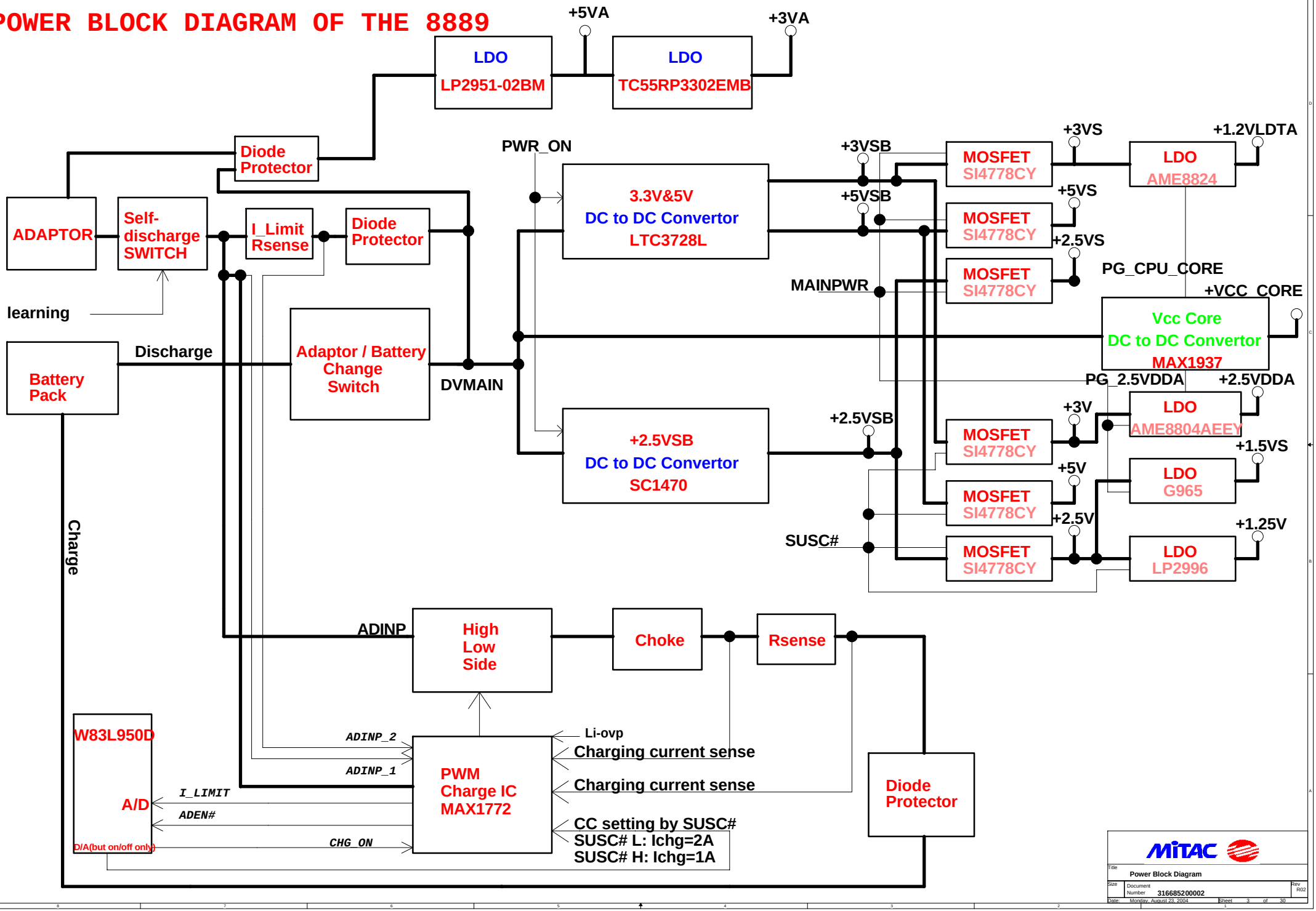
# 8889 SYSTEM BLOCK DIAGRAM




MiTAC

| | | |
|---|---|---|
| Title | System Block DIAGRAM | |
| Size | Document Number 316685200002 | Rev R02 |
| Date: Monday, August 23, 2004 | Sheet 2 of 30 | |

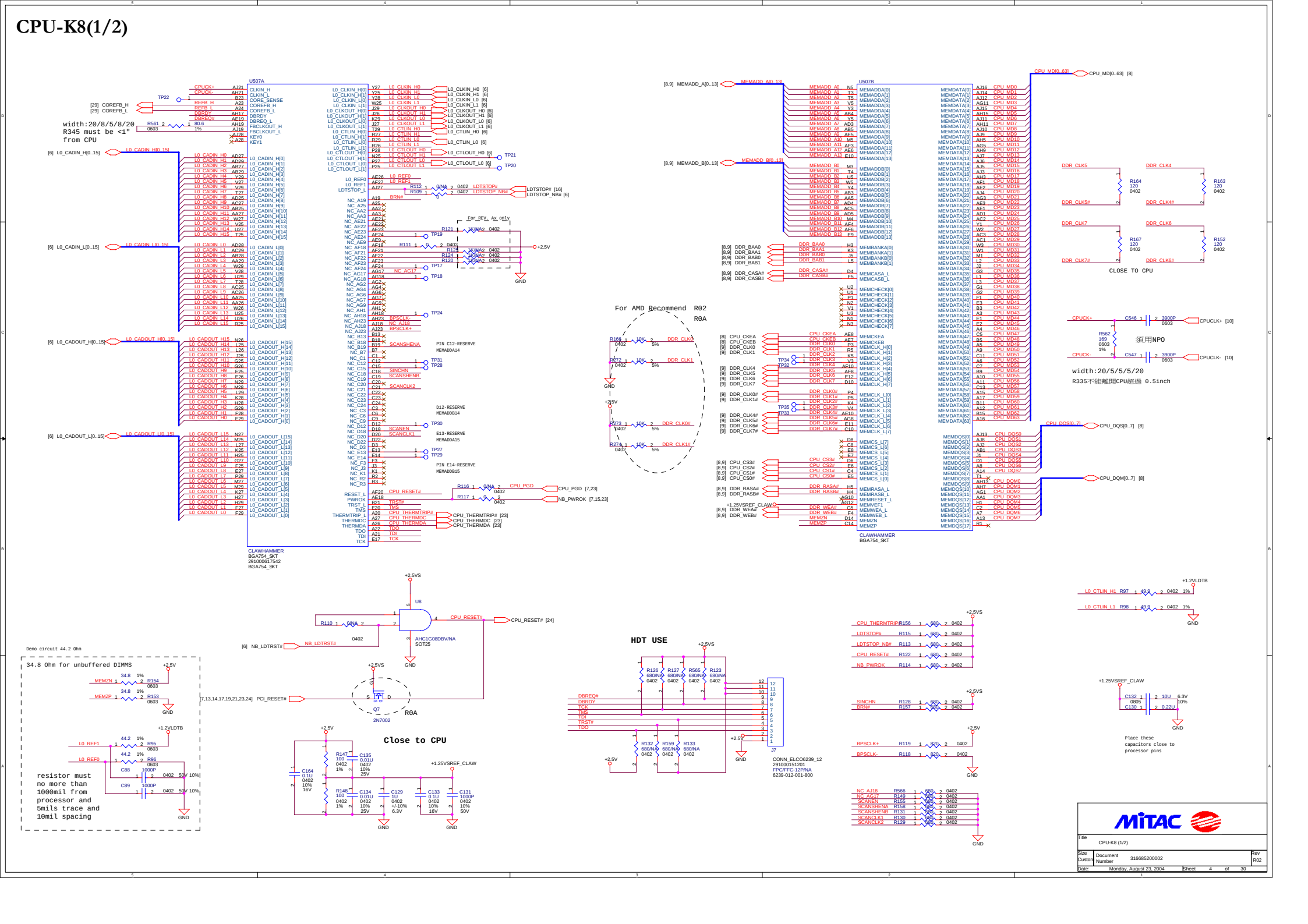
# POWER BLOCK DIAGRAM OF THE 8889




MiTAC

| | | |
|---|---|---|
| Title | Power Block Diagram | |
| Size | Document Number 316685200002 | Rev R02 |
| Date: Monday, August 23, 2004 | Sheet 3 of 30 | |

# CPU-K8(1/2)


U507A
CLAWHAMMER
BGA754_SKT
291000617542
U507B
CLAWHAMMER
BGA754_SKT
width:20/8/5/8/20
R345 must be <1"
from CPU
For AMD Recommend R02
R0A
須用NPO
width:20/5/5/5/20
R335不能離開CPU超過 0.5inch
CLOSE TO CPU
HDT USE
Close to CPU
34.8 Ohm for unbuffered DIMMS
resistor must
no more than
1000mil from
processor and
5mils trace and
10mil spacing
Demo circuit 44.2 Ohm
Place these
capacitors close to
processor pins
CONN_ELCO6239_12
291000151201
FPC/FFC-12P/NA
6239-012-001-800
MiTAC
Title
CPU-K8 (1/2)
Size
Custom
Document Number
316685200002
Rev
R02
Date:
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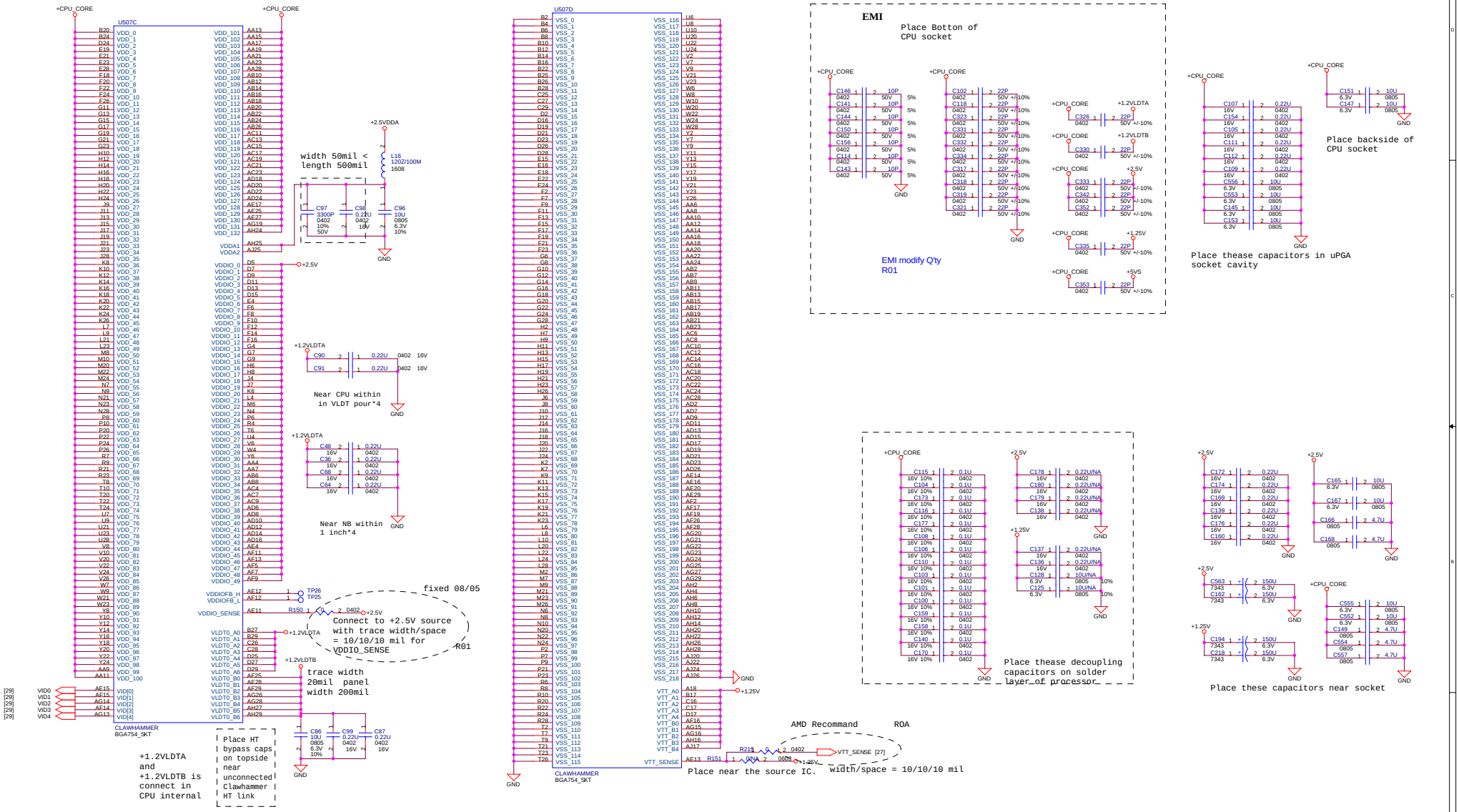
4
of
30

# CPU-K8 (2/2)




| | |
|---|---|
| Title | CPU-K8 (2/2) |
| Size | Custom |
| Document Number | 316685200002 |
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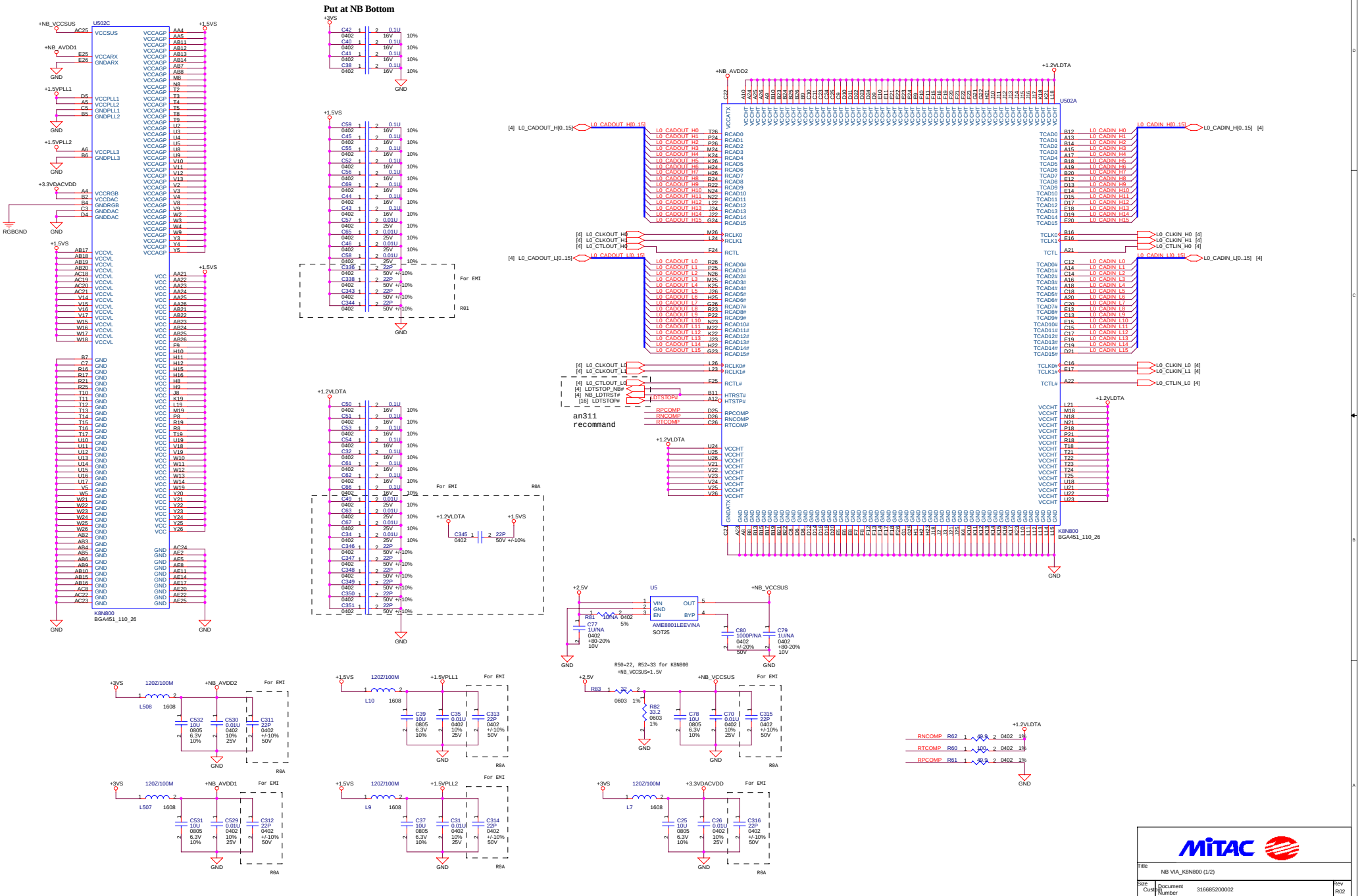
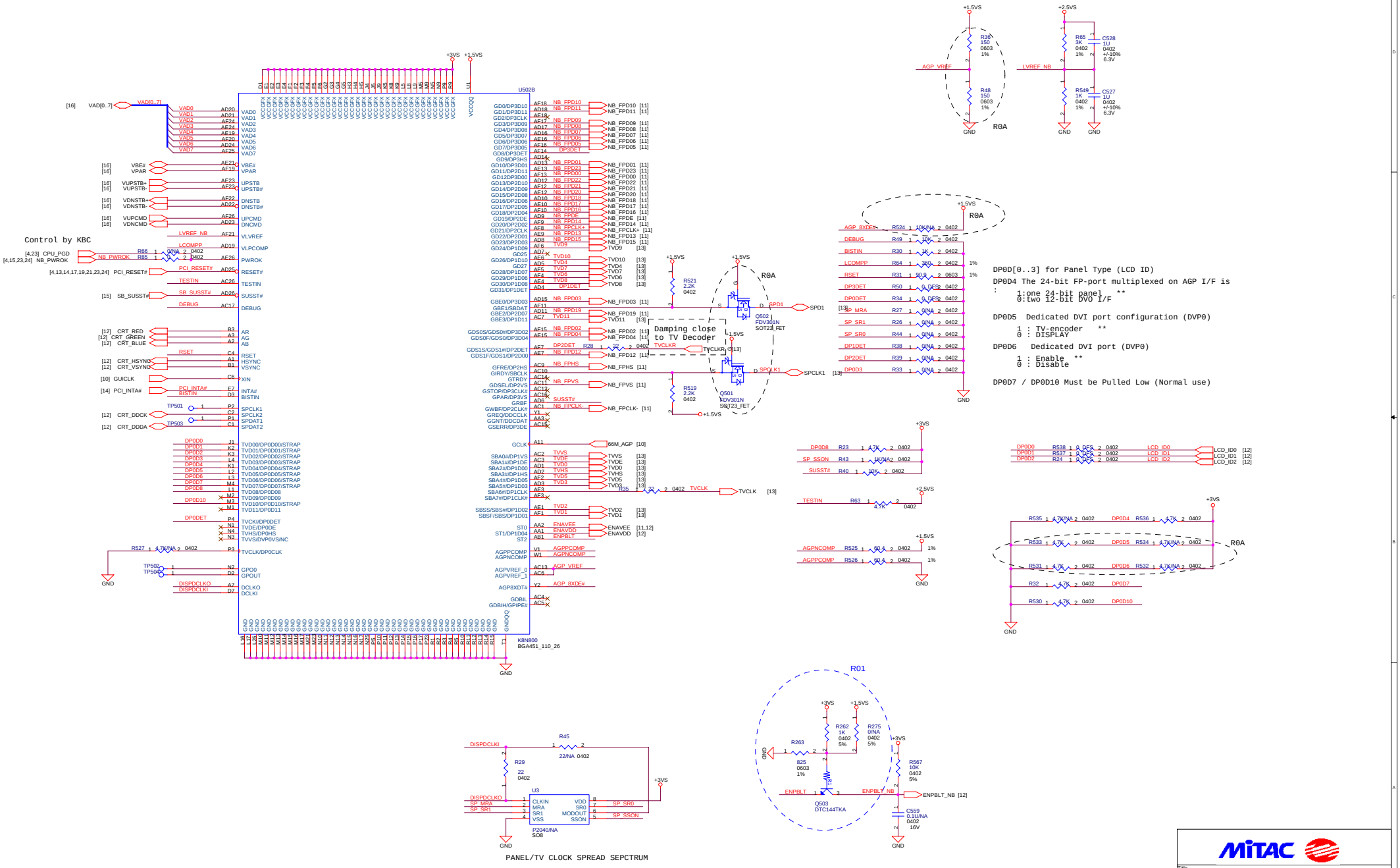
| Date: | Monday, August 23, 2004 |
| Sheet | 5 of 30 |

# NB VIA_K8N800 (1/2)

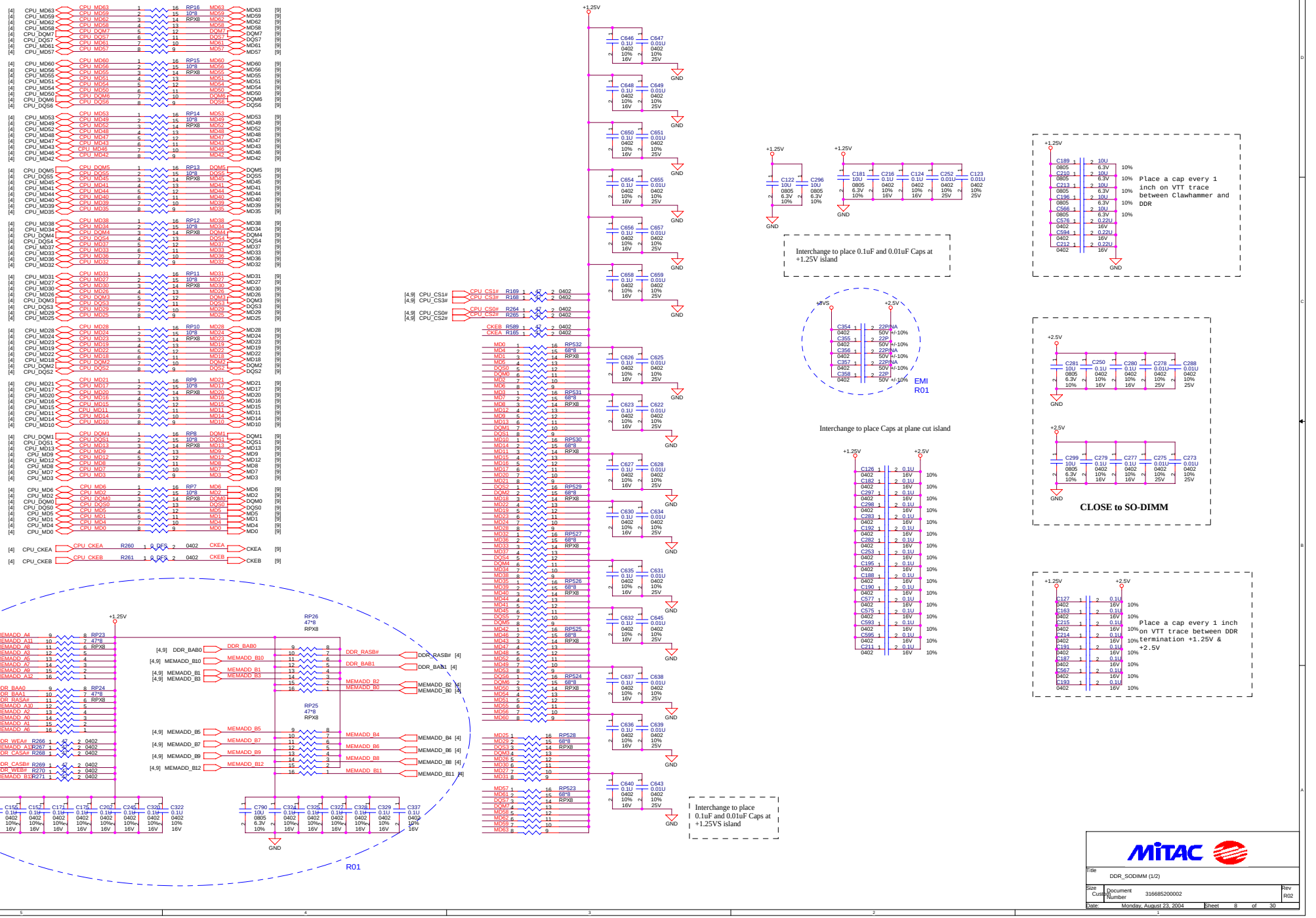


# NB VIA_K8N800 (2/2)



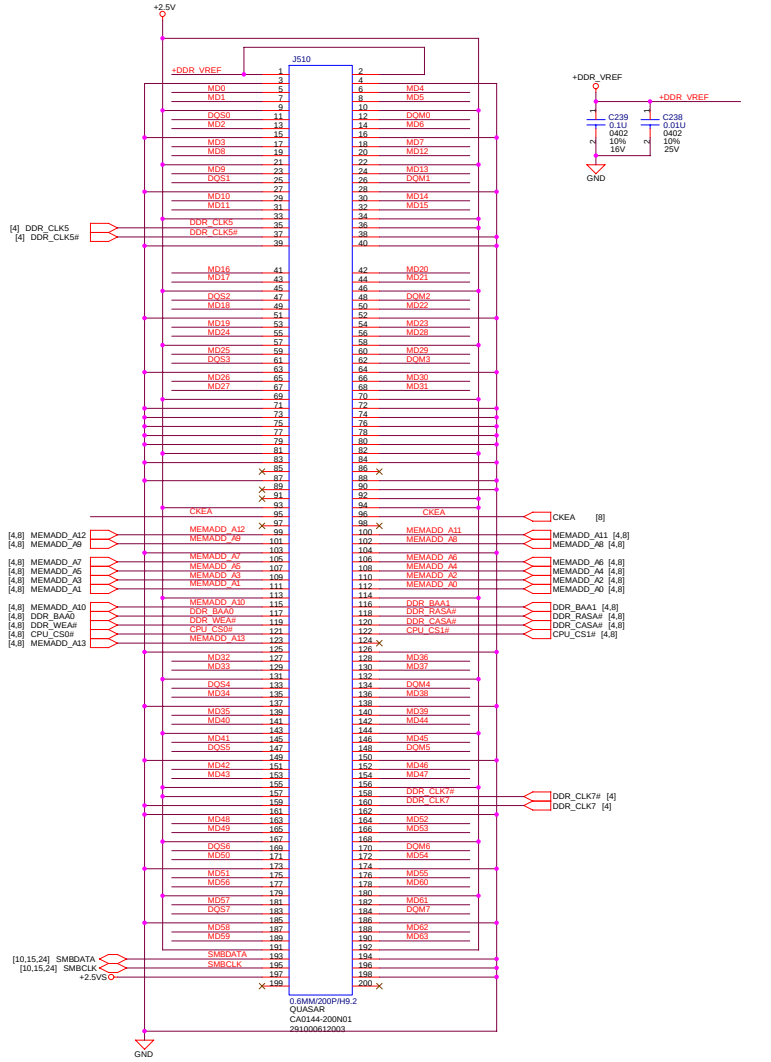

| | | | |
|---|---|---|---|
| Title | NB VIA_K8N800 (2/2) | | |
| Size | Document Number | 316685200002 | Rev R02 |
| Custom | | | |
| Date: | Monday, August 23, 2004 | Sheet 7 of 30 | |

# DDR_SODIMM(1/2)

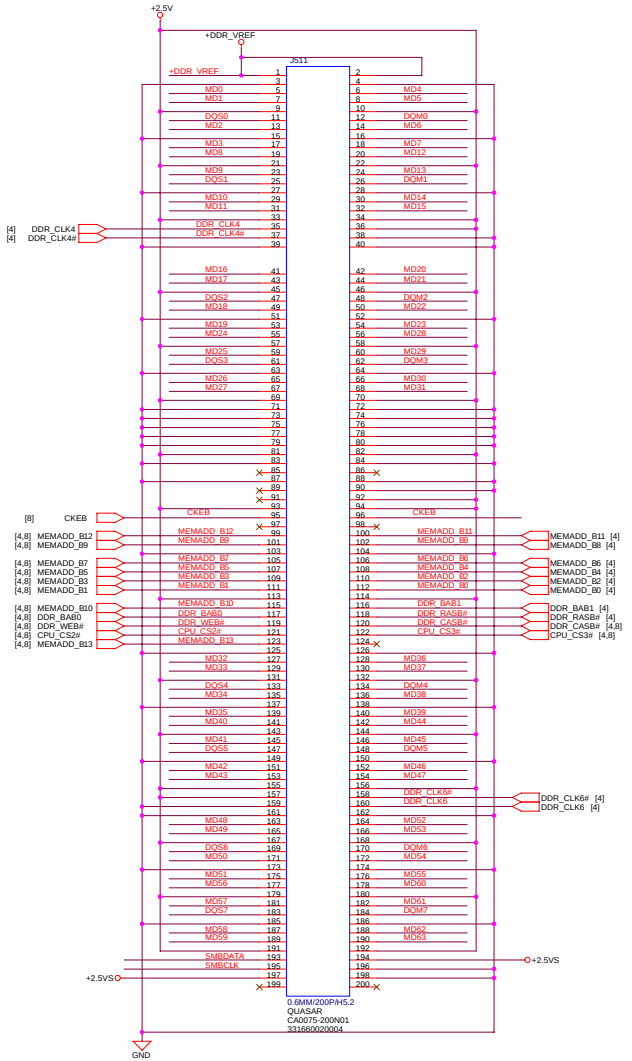

Interchange to place 0.1uF and 0.01uF Caps at +1.25V island
Interchange to place Caps at plane cut island
Place a cap every 1 inch on VTT trace between Clawhammer and DDR
Place a cap every 1 inch on VTT trace between DDR termination +1.25V & +2.5V
CLOSE to SO-DIMM
EMI
R01

| | |
|---|---|
| Title | DDR_SODIMM (1/2) |
| Size | Custom |
| Document Number | 316685200002 |
| Rev | R02 |
| Date: | Monday, August 23, 2004 |
| Sheet | 8 of 30 |

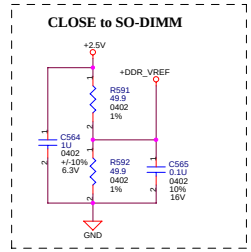
# DDR_SODIMM(2/2)

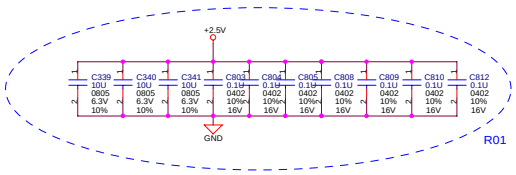



I2C / SMB Address : A0h

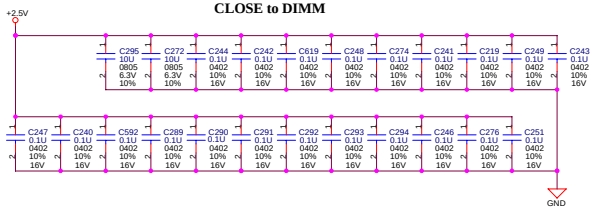



I2C / SMB Address : A2h




CLOSE to DIMM

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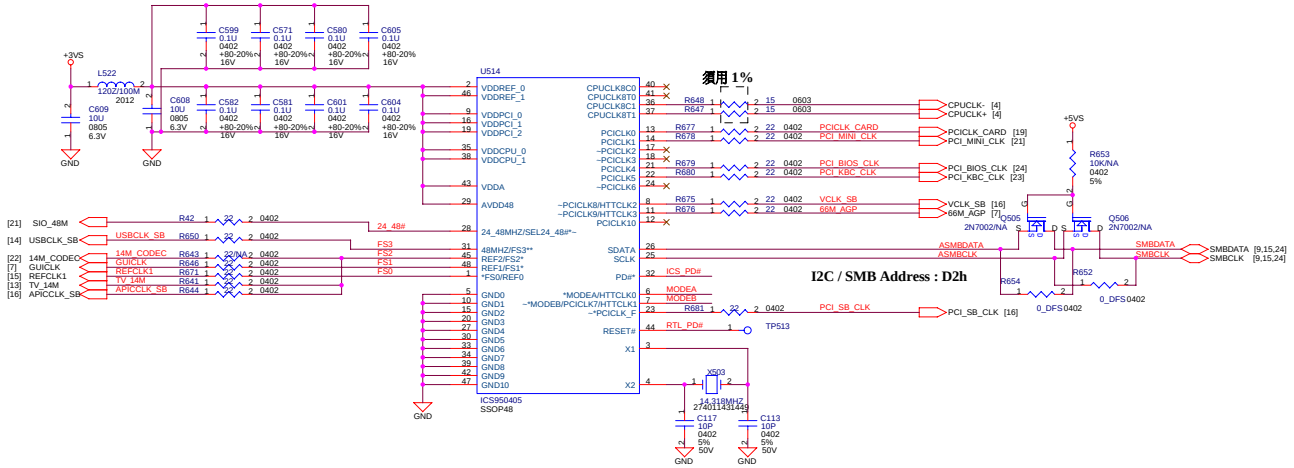
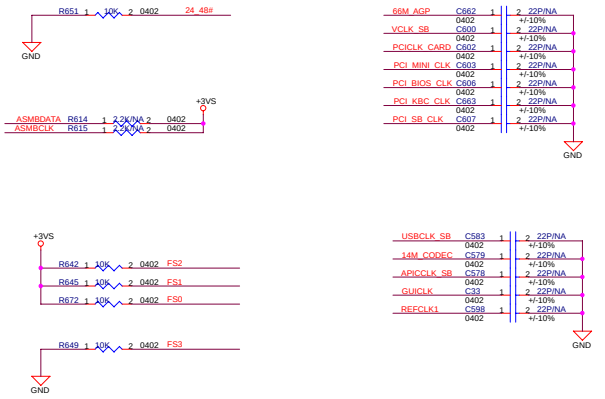
| | | |
|---|---|---|
| Title | DDR_SODIMM (2/2) | |
| Size: Custom | Document Number: 316685200002 | Rev: R02 |
| Date: Monday, August 23, 2004 | Sheet 9 of 30 | |

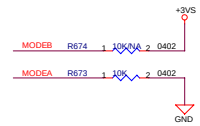
# CLOCK GENERATOR(ICS950405)



## MODE FUNCTIONALITY TABLES

| MODE A | MODE B | Pin6 | Pin7 | Pin8 | Pin11 | |
|---|---|---|---|---|---|---|
| 0 | 0 | 66MHZ | 66MHZ | 66MHZ | 33MHZ | |
| 0 | 1 | MODE A INPUT ONLY | 66MHZ | 66MHZ | 66MHZ | **DEFAULT** |
| 1 | 0 | 33MHZ | 33MHZ | 33MHZ | 33MHZ | |
| 1 | 1 | MODE A INPUT ONLY | 33MHZ | 33MHZ | 33MHZ | |



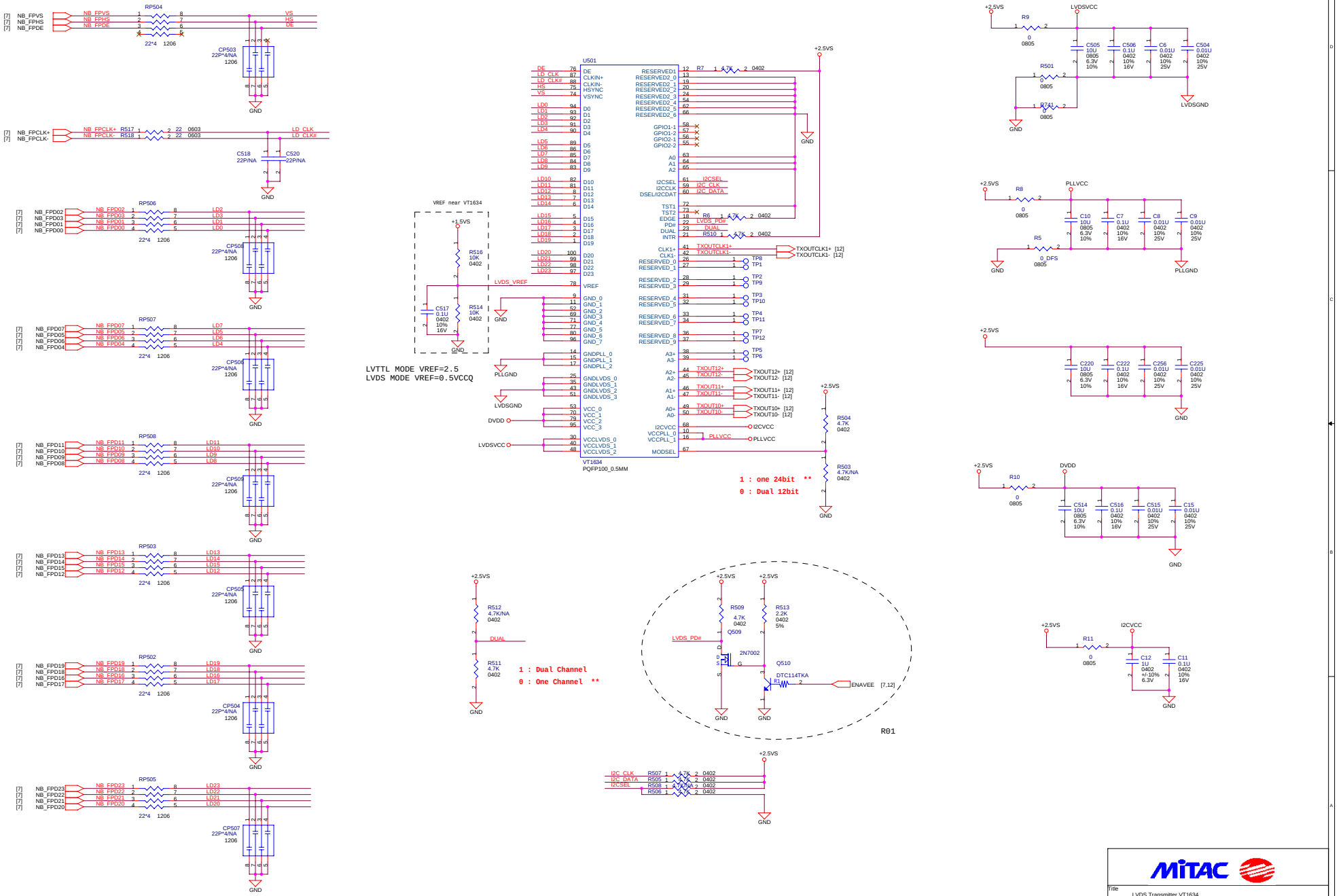




| FS3 | FS2 | FS1 | FS0 | CPU Mhz | HTT Mhz | PCI Mhz | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 100.90 | 67.27 | 33.63 | |
| 0 | 0 | 0 | 1 | 133.90 | 66.95 | 33.48 | |
| 0 | 0 | 1 | 0 | 168.00 | 67.20 | 33.60 | |
| 0 | 0 | 1 | 1 | 202.00 | 67.33 | 33.67 | |
| 0 | 1 | 0 | 0 | 100.20 | 66.80 | 33.40 | |
| 0 | 1 | 0 | 1 | 133.50 | 66.75 | 33.38 | |
| 0 | 1 | 1 | 0 | 166.70 | 67.68 | 33.34 | |
| 0 | 1 | 1 | 1 | 200.40 | 66.80 | 33.40 | **DEFAULT** |
| 1 | 0 | 0 | 0 | 150.00 | 60.00 | 33.00 | |
| 1 | 0 | 0 | 1 | 180.00 | 60.00 | 33.00 | |
| 1 | 0 | 1 | 0 | 210.00 | 70.00 | 35.00 | |
| 1 | 0 | 1 | 1 | 240.00 | 60.00 | 30.00 | |
| 1 | 1 | 0 | 0 | 270.00 | 67.50 | 33.75 | |
| 1 | 1 | 0 | 1 | 233.33 | 66.67 | 33.33 | |
| 1 | 1 | 1 | 0 | 266.67 | 66.67 | 33.33 | |
| 1 | 1 | 1 | 1 | 300.00 | 75.00 | 37.50 | |

MiTAC

| | | |
|---|---|---|
| Title | Clock Generator | |
| Size: Custom | Document Number: 316685200002 | Rev: R02 |
| Date: Monday, August 23, 2004 | Sheet 10 of 30 | |

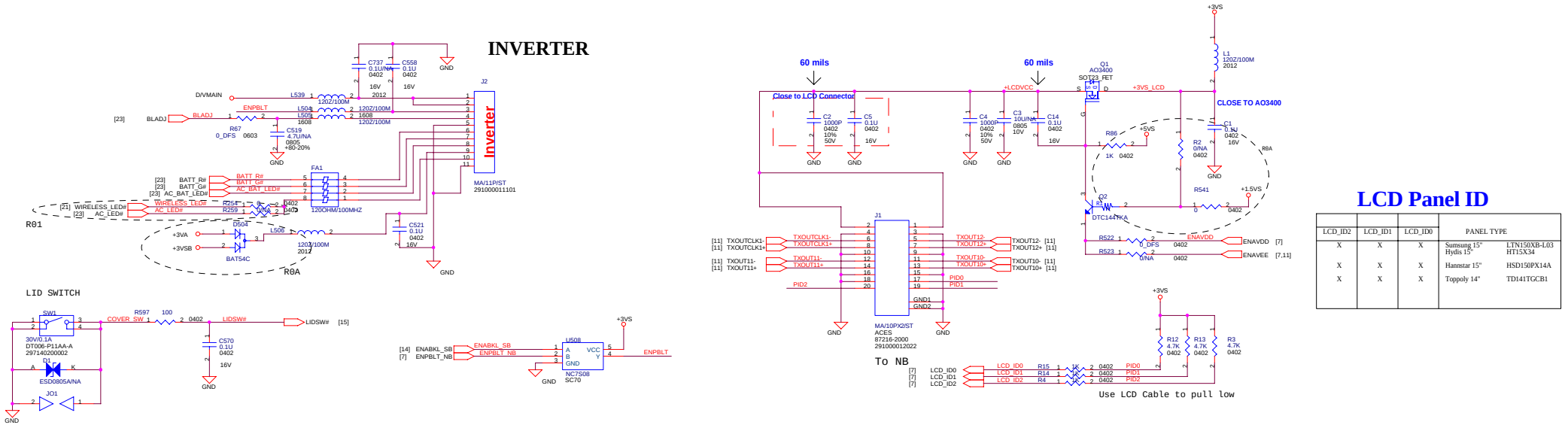
# VT1634 LVDS Transmitter




MiTAC

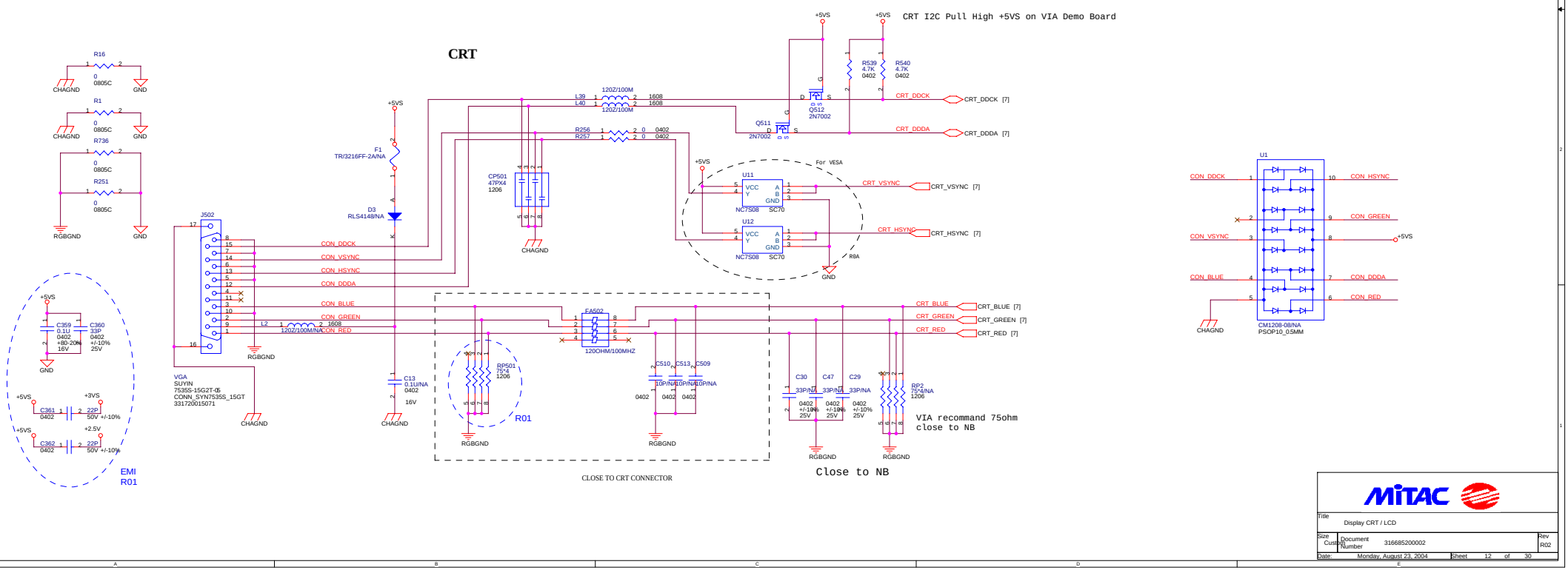
| | |
|---|---|
| Title | LVDS Transmitter VT1634 |
| Size: Custom | Document Number: 316685200002 |
| Rev | R02 |
| Date: Monday, August 23, 2004 | Sheet 11 of 30 |

# Display (CRT / LCD)



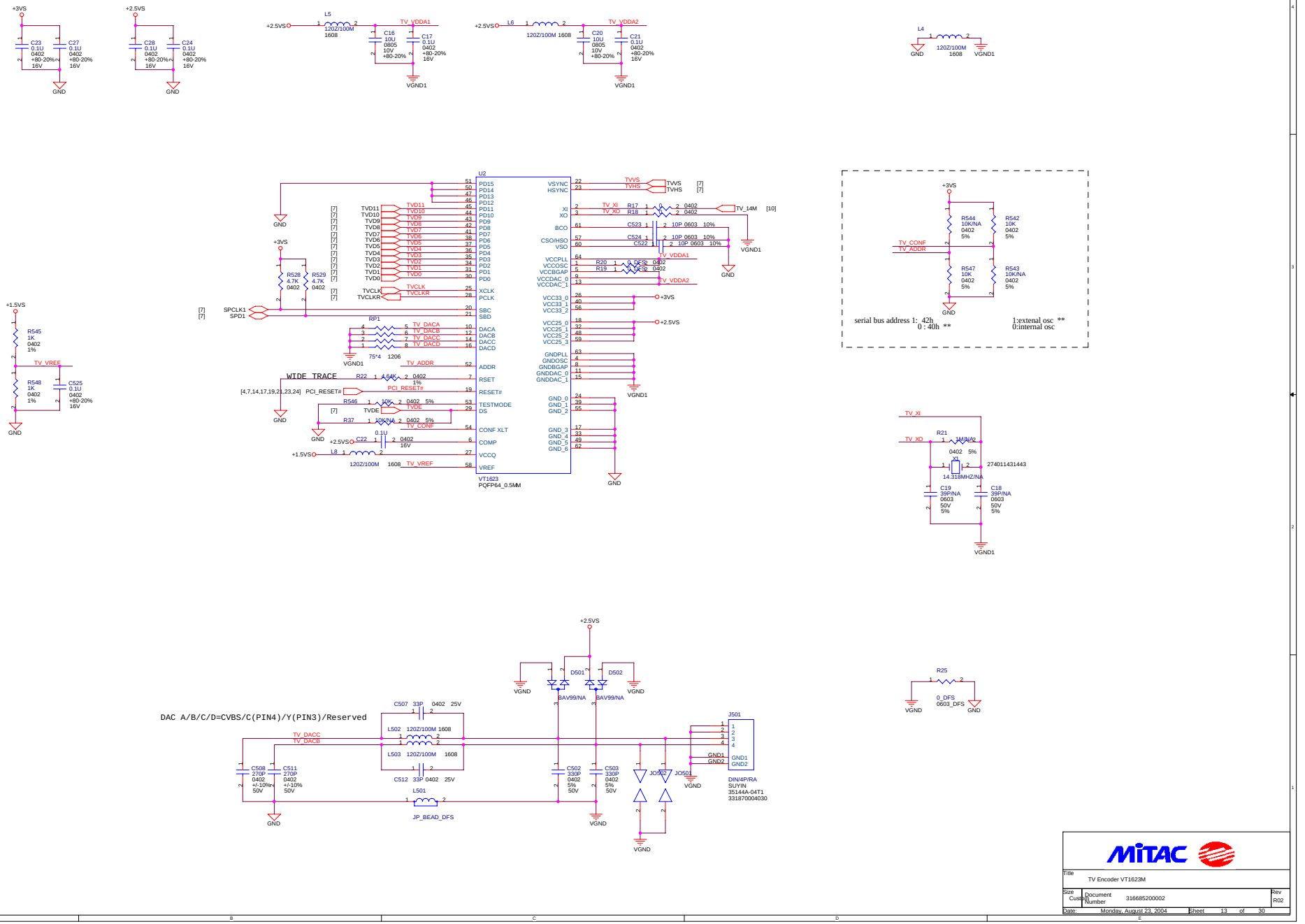

## LCD Panel ID

| LCD_ID2 | LCD_ID1 | LCD_ID0 | PANEL TYPE | |
|---|---|---|---|---|
| X | X | X | Sumsung 15" | LTN150XB-L03 |
| | | | Hydis 15" | HT15X34 |
| X | X | X | Hannstar 15" | HSD150PX14A |
| X | X | X | Toppoly 14" | TD141TGCB1 |



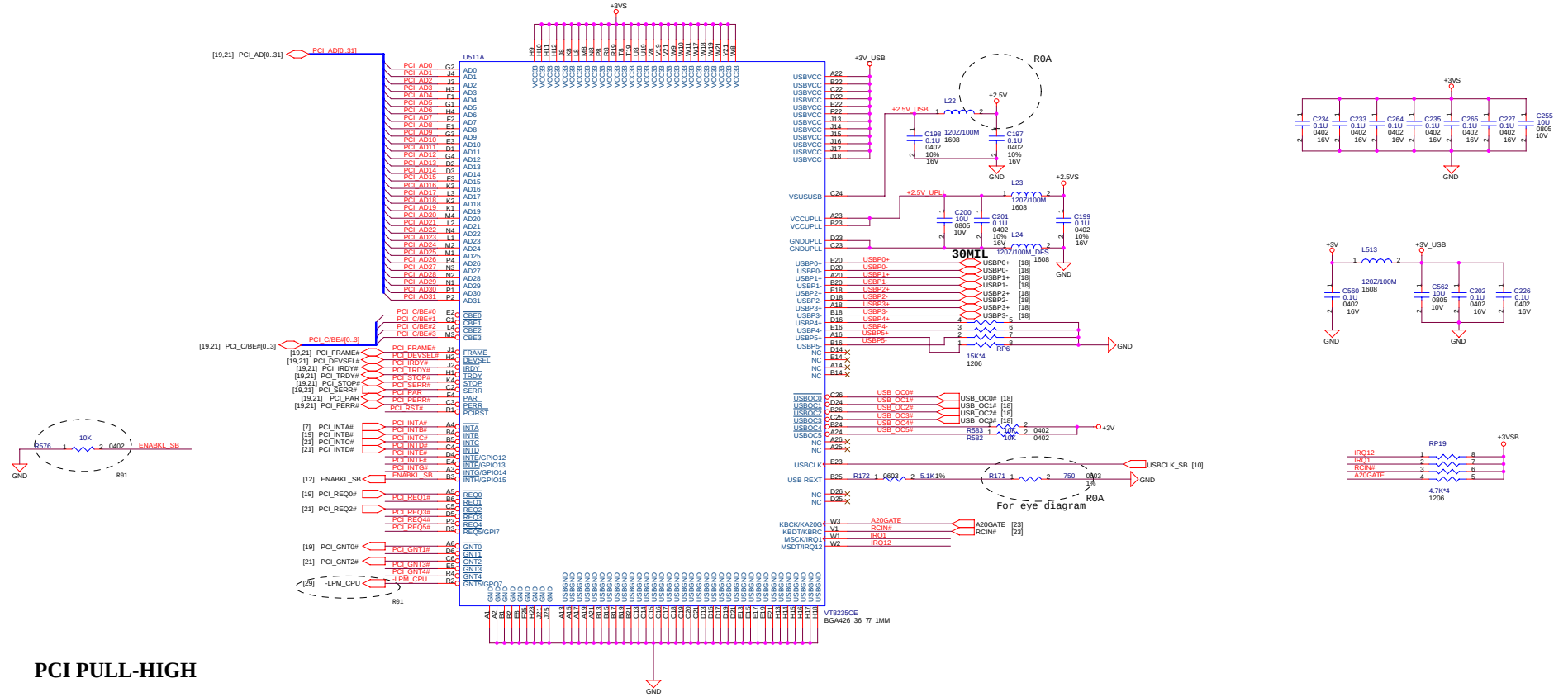

| | | | |
|---|---|---|---|
| Title | Display CRT / LCD | | |
| Size: Custom | Document Number: 316685200002 | | Rev: R02 |
| Date: Monday, August 23, 2004 | Sheet 12 of 30 | | |

# Display (TV Encoder)



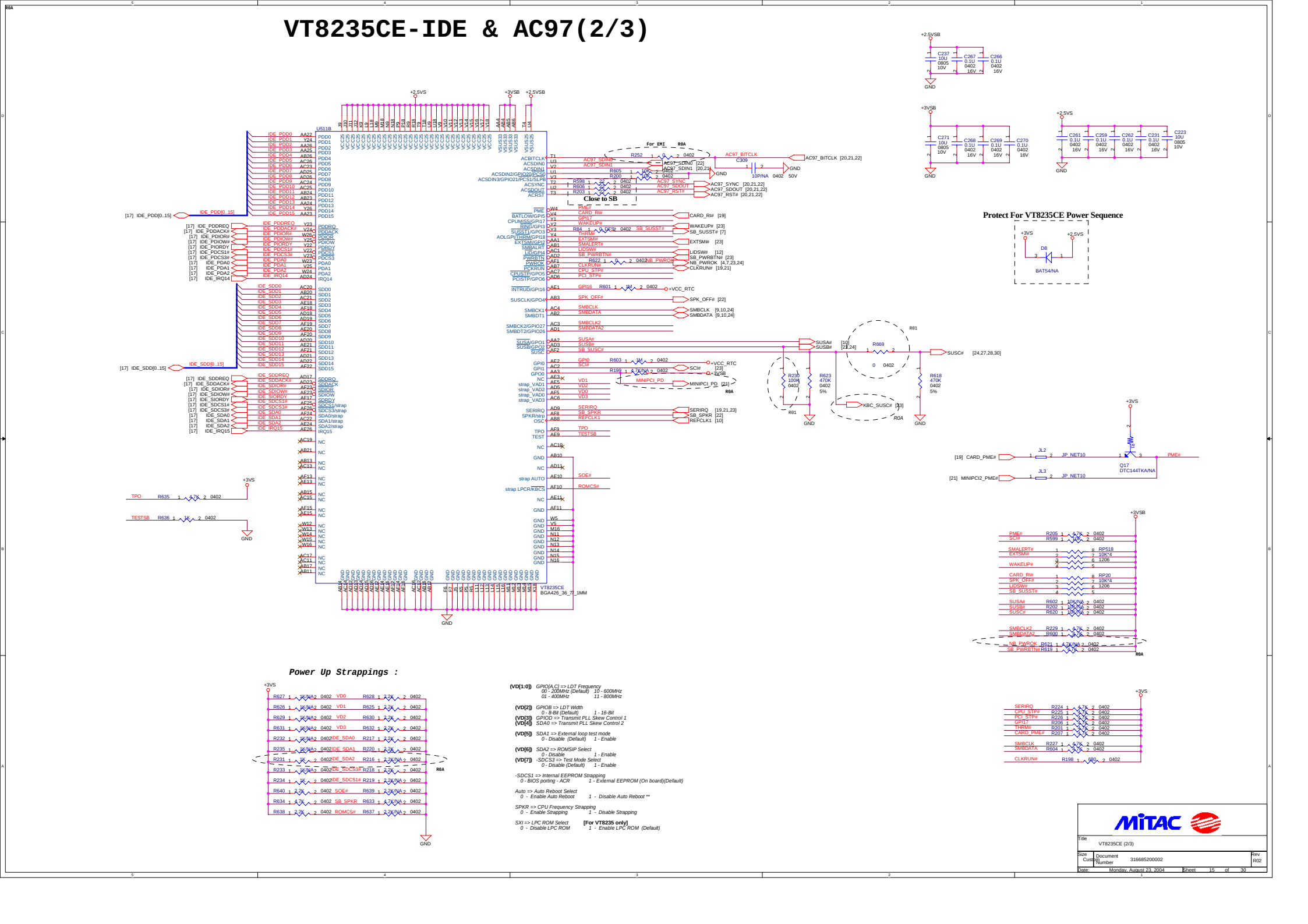

| | |
|---|---|
| Title | TV Encoder VT1623M |
| Size: Custom | Document Number: 316685200002 |
| Rev | R02 |
| Date: | Monday, August 23, 2004 |
| Sheet | 13 of 30 |

# VT8235CE- PCI & USB(1/3)




| | |
|---|---|
| Title | VT8235CE (1/3) |
| Size | Custom |
| Document Number | 316685200002 |
| Rev | R02 |
| Date: | Monday, August 23, 2004 |
| Sheet | 14 of 30 |

# VT8235CE-IDE & AC97(2/3)


U51B
VT8235CE
BGA426_36_77_1MM
Close to SB
For EMI
R0A
Protect For VT8235CE Power Sequence
BAT54/NA
Power Up Strappings :
(VD[1:0]) GPIO[A,C] => LDT Frequency
00 - 200MHz (Default) 10 - 600MHz
01 - 400MHz 11 - 800MHz
(VD[2]) GPIOB => LDT Width
0 - 8-Bit (Default) 1 - 16-Bit
(VD[3]) GPIOD => Transmit PLL Skew Control 1
(VD[4]) SDA0 => Transmit PLL Skew Control 2
(VD[5]) SDA1 => External loop test mode
0 - Disable (Default) 1 - Enable
(VD[6]) SDA2 => ROMSIP Select
0 - Disable 1 - Enable
(VD[7]) -SDCS3 => Test Mode Select
0 - Disable (Default) 1 - Enable
-SDCS1 => Internal EEPROM Strapping
0 - BIOS porting - ACR 1 - External EEPROM (On board)(Default)
Auto => Auto Reboot Select
0 - Enable Auto Reboot 1 - Disable Auto Reboot **
SPKR => CPU Frequency Strapping
0 - Enable Strapping 1 - Disable Strapping
SXI => LPC ROM Select [For VT8235 only]
0 - Disable LPC ROM 1 - Enable LPC ROM (Default)
MiTAC
Title
VT8235CE (2/3)
Size
Custom
Document Number
316685200002
Rev
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Date:
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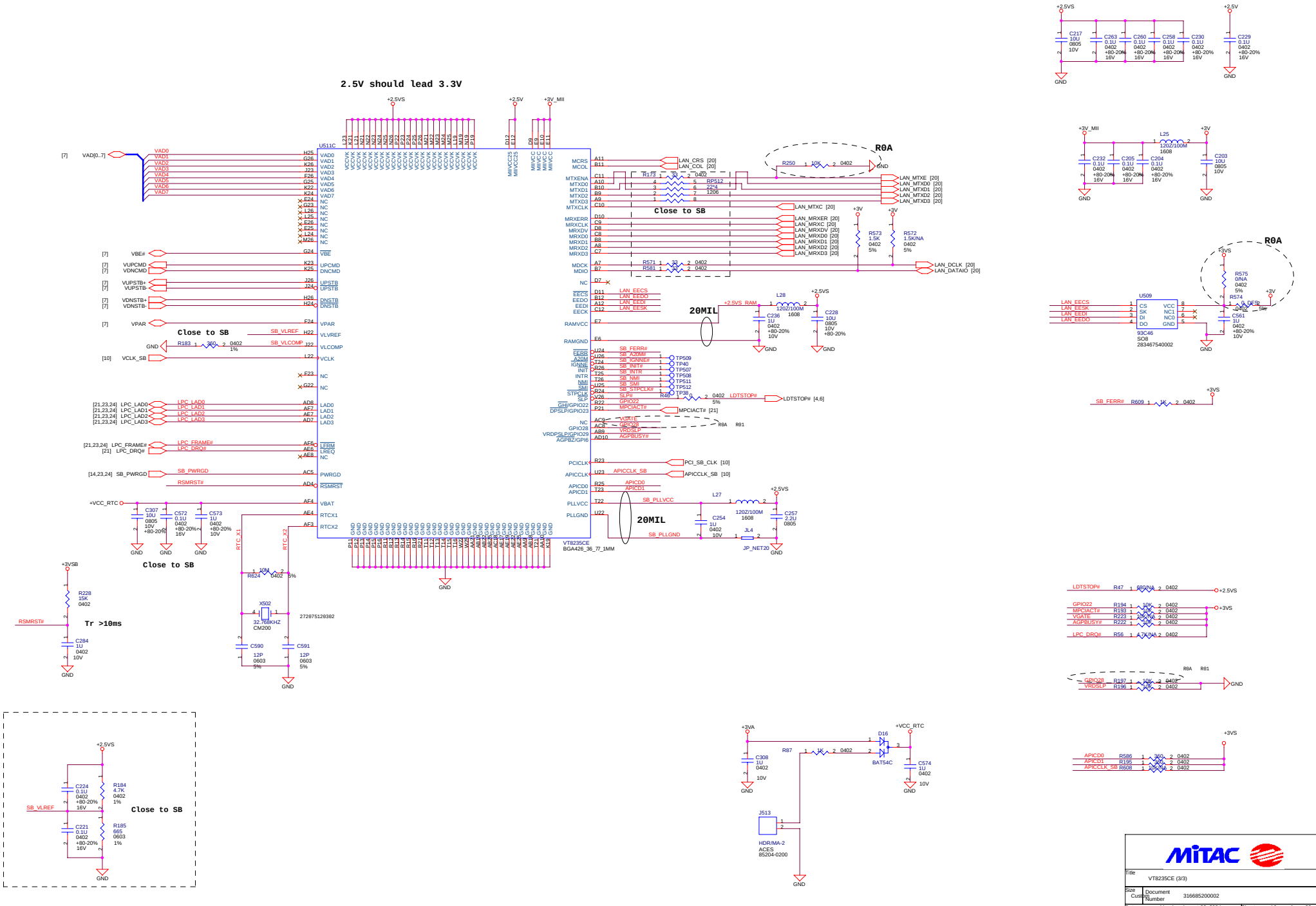
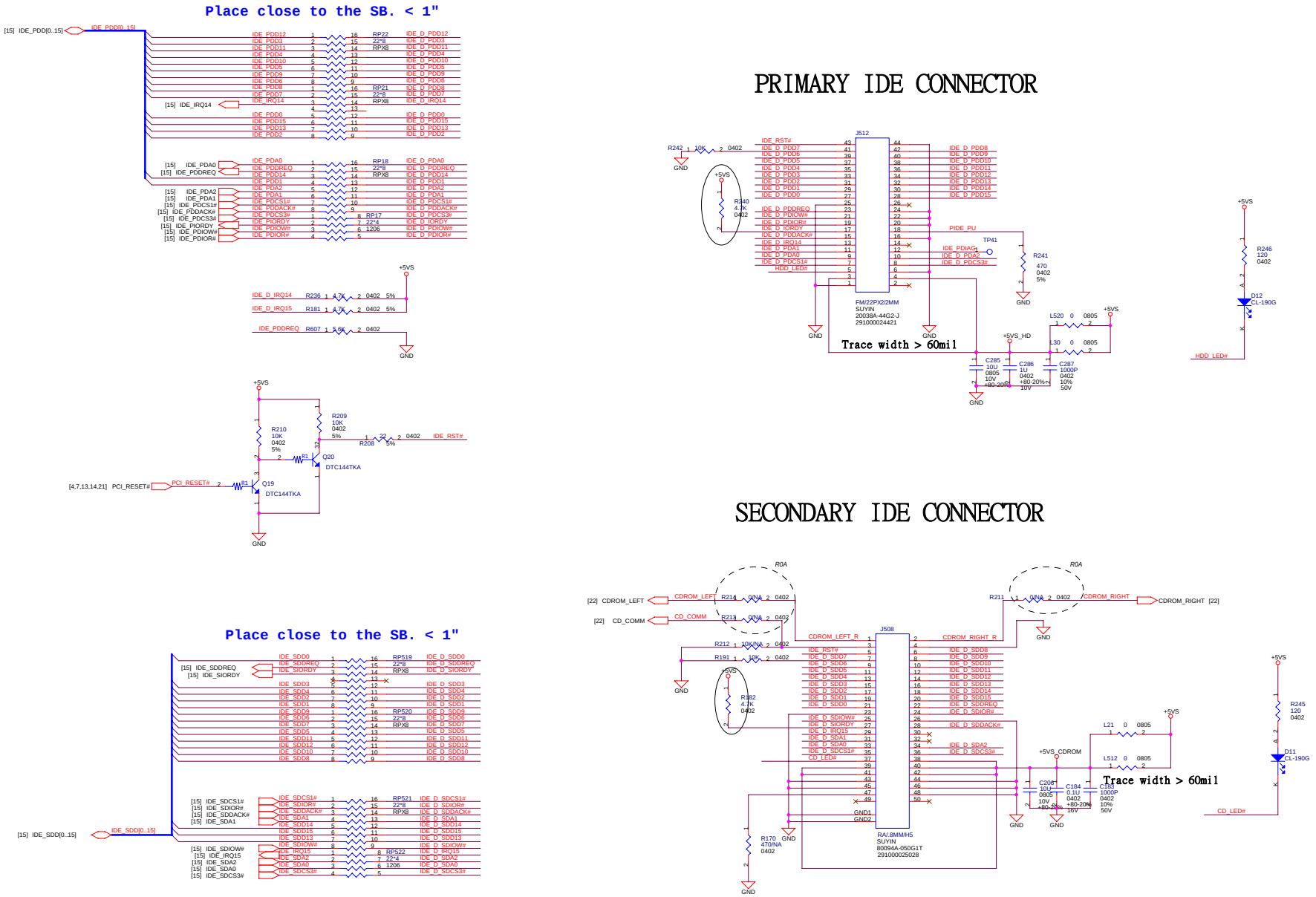
# VT8235CE-VLINK& LAN(3/3)






| | |
|---|---|
| Title | IDE INTERFACE |
| Size / Custom | Document Number 316685200002 |
| Rev | R02 |
| Date: | Monday, August 23, 2004 |
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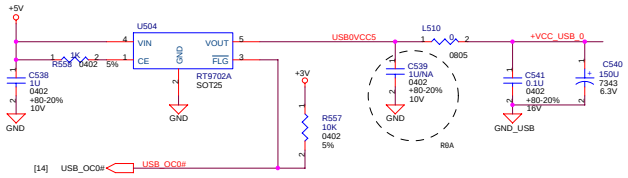
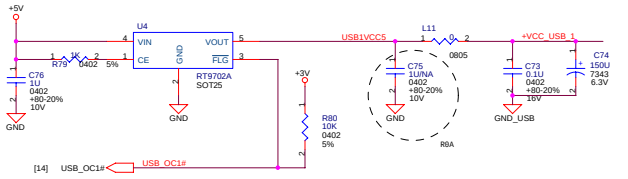
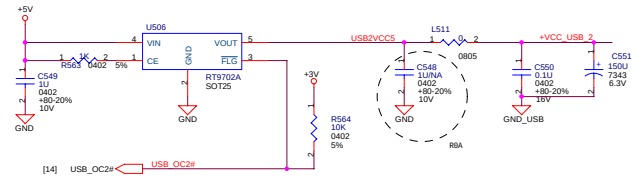
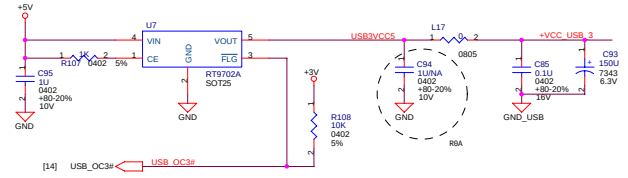
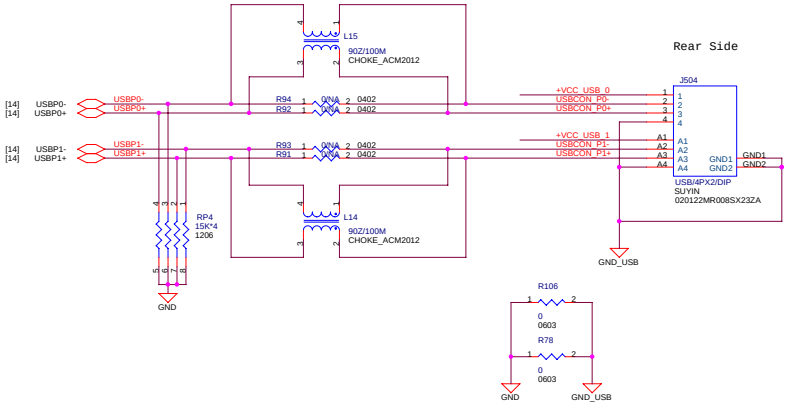
# USB CONNECOTR

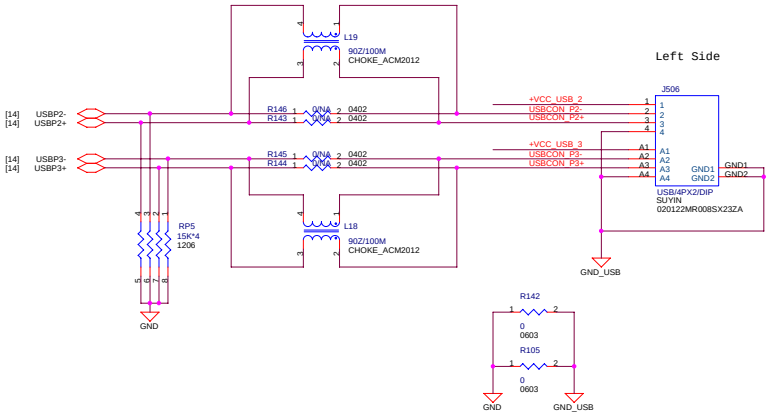



MiTAC

| | | |
|---|---|---|
| Title | USB | |
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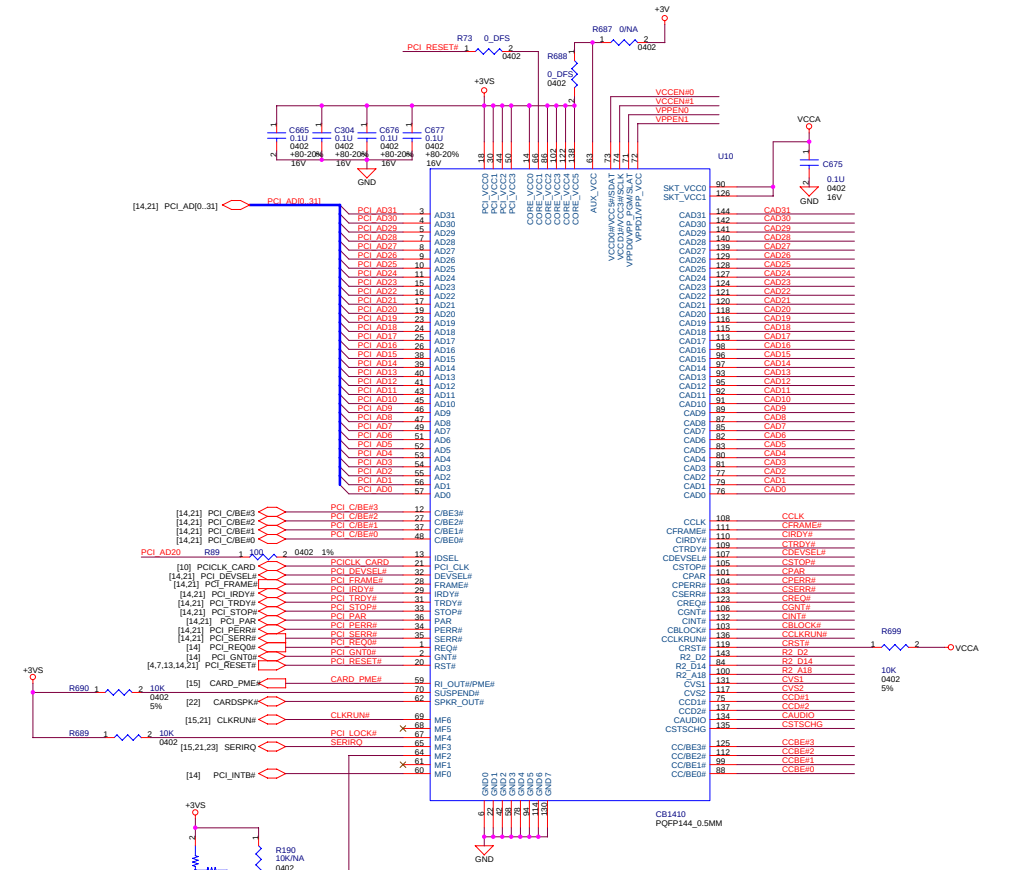
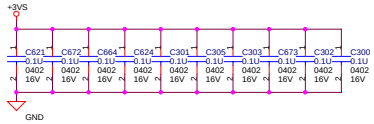
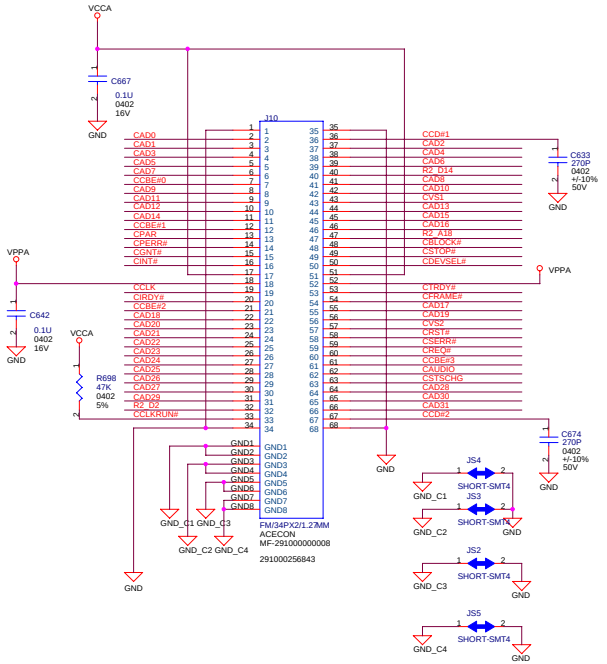
| Date: Monday, August 23, 2004 | Sheet 18 of 30 | |

**ENE CB1410**

AD20
PCI_INTB# (Card BUS)
REQ0#/GNT0#

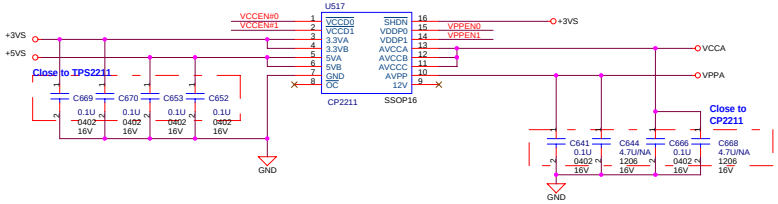




VCCA
C667 0.1U 0402 16V
J10
CAD0 CAD1 CAD3 CAD5 CAD7 CCBE#0 CAD9 CAD11 CAD12 CAD14 CCBE#1 CPAR CPERR# CGNT# CINT#
CCLK CIRDY# CCBE#2 CAD18 CAD20 CAD21 CAD22 CAD23 CAD24 CAD26 CAD27 CAD29 R2_D2 CCLKRUN#
CCD#1 CAD2 CAD4 CAD6 R2_D14 CAD8 CAD10 CVS1 CAD13 CAD15 CAD16 R2_A18 CBLOCK# CSTOP# CDEVSEL#
CTRDY# CFRAME# CAD17 CAD19 CVS2 CRST# CSERR# CREQ# CCBE#3 CAUDIO CSTSCHG CAD28 CAD30 CAD31 CCD#2
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8
FM/34PX2/1.27MM
ACECON
MF-291000000008
291000256843
C633 270P 0402 +/-10% 50V
C674 270P 0402 +/-10% 50V
VPPA
C642 0.1U 0402 16V
R698 47K 0402 5%
GND_C1 GND_C3
GND_C2 GND_C4
JS4 JS3 JS2 JS5
SHORT-SMT4

| SIGNAL | PC CARD PULL UP | VOLT |
|---|---|---|
| CCD#1 | +3V | |
| CCD#2 | +3V | |
| CBLOCK# | CARD_VCC | |
| CSTOP# | CARD_VCC | |
| CDEVSEL# | CARD_VCC | |
| CTRDY# | CARD_VCC | |
| CVS1 | +3V | |
| CVS2 | +3V | |
| CRST# | CARD_VCC | |
| CSERR# | CARD_VCC | |
| CPERR# | CARD_VCC | |
| CINT# | CARD_VCC | |
| CIRDY# | CARD_VCC | |
| CREQ# | CARD_VCC | |
| CSTSCHG# | CARD_VCC | |
| CAUDIO | CARD_VCC | |

PCI1410 HAVE INTEGRATED ALL PULL UP RES ABOVE




| | | |
|---|---|---|
| Title | ENE CB1410 | |
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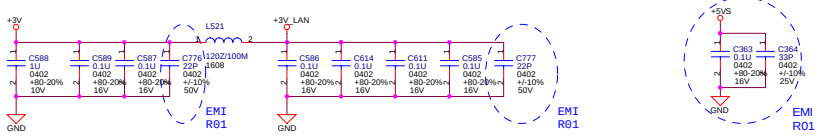
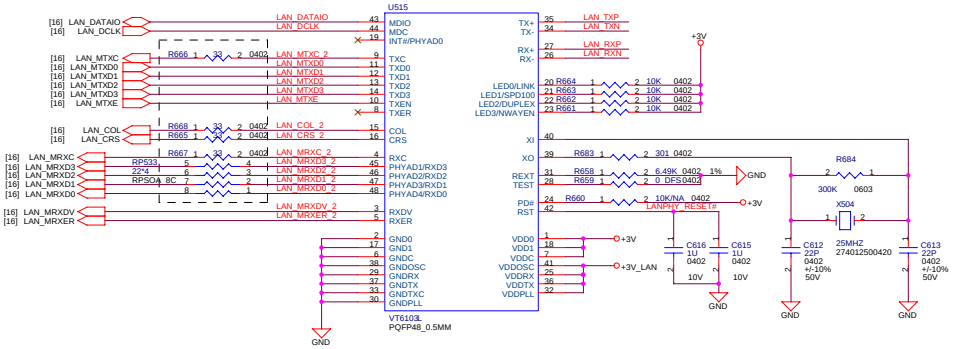
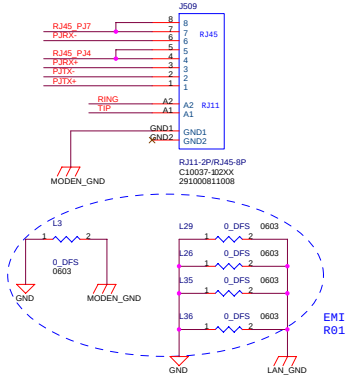
# LAN (PHY-VT6103) & MDC




Close to VT6103L PHY

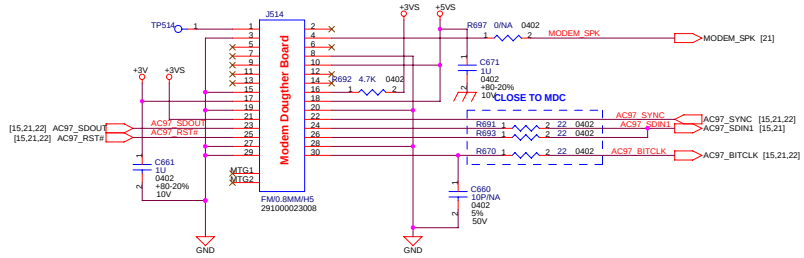



## RJ45 / RJ11 CONNECTOR




## MDC

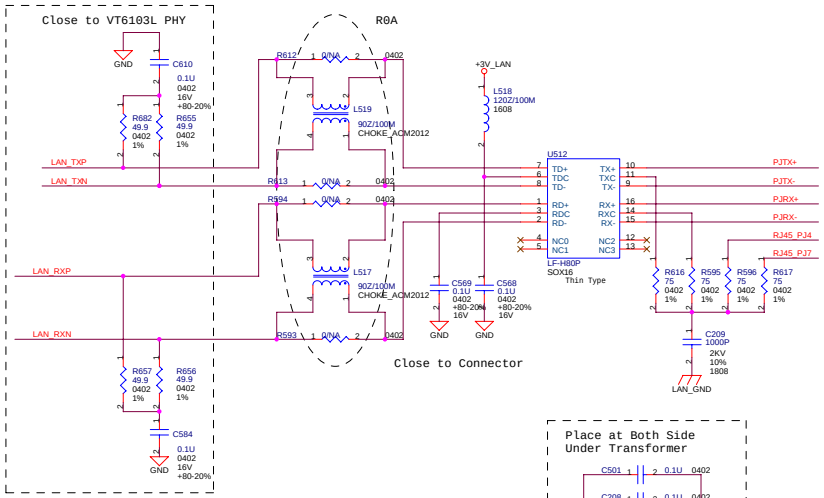
### AC-Link



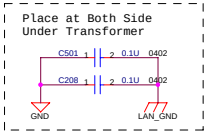

Change 90Z choke for EMI

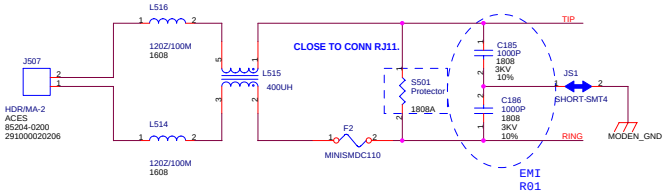
R0A

Close to VT6103L PHY




Place at Both Side Under Transformer




| | | | |
|---|---|---|---|
| MiTAC | | | |
| Title | LAN (VT6103) & MDC | | |
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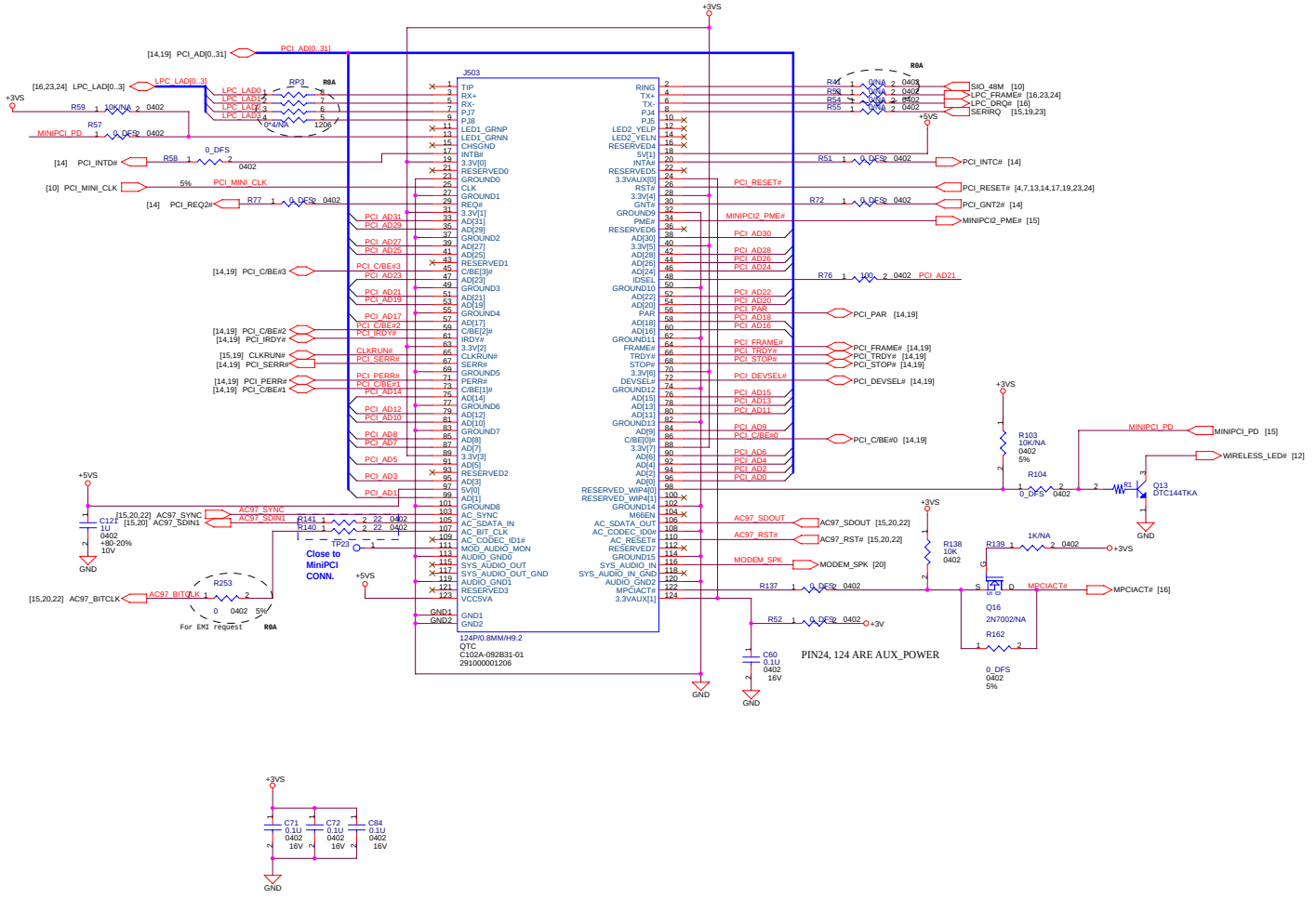
**MINI-PCI**
AD19
PCI_INTD#
(PCI_INTC#)
REQ2#/GNT2#

# MINI-PCI (Wireless)




| | | | |
|---|---|---|---|
| Title | MINI PCI (Wireless) | | |
| Size: Custom | Document Number: 316685200002 | | Rev: R02 |
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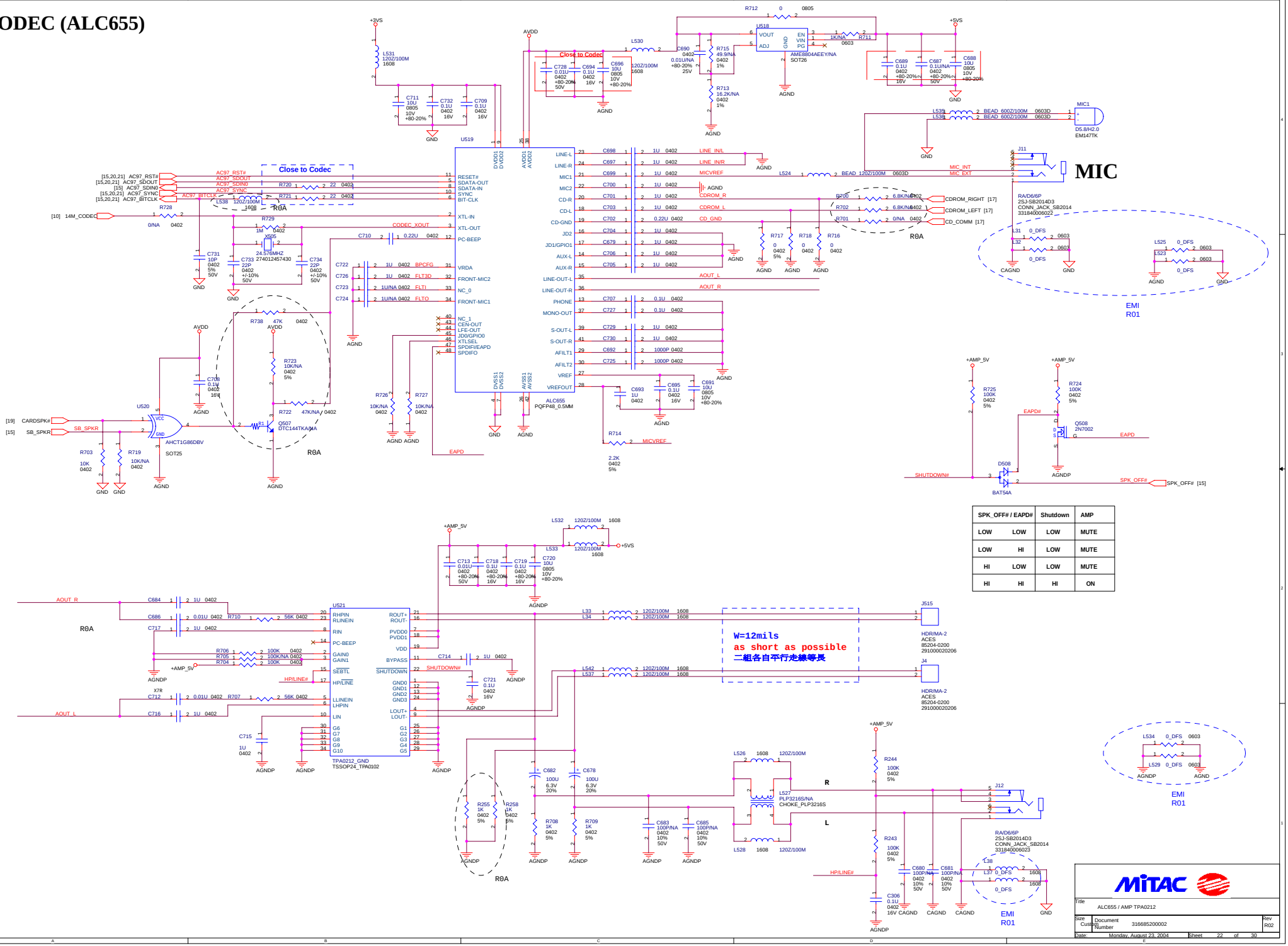
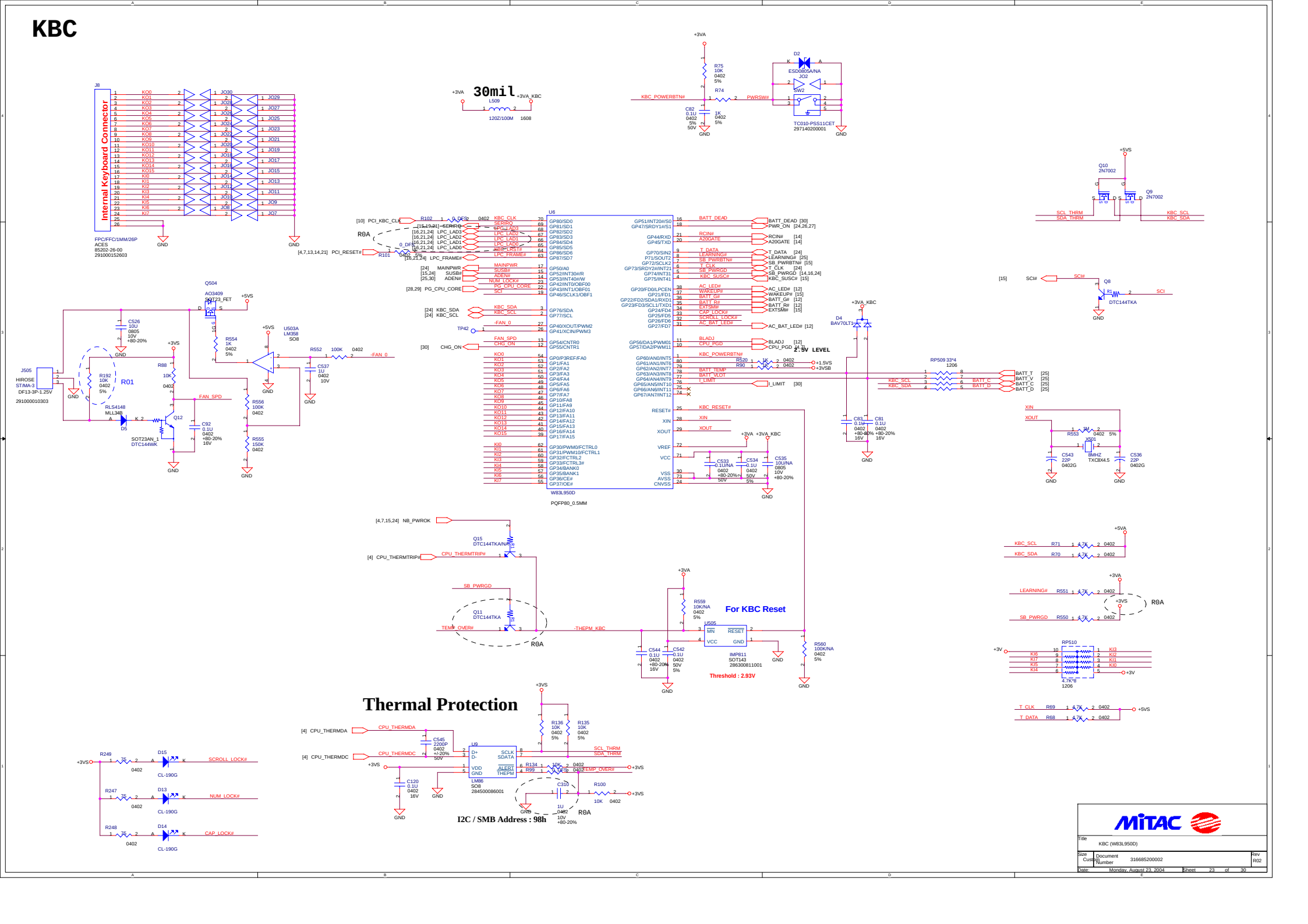
# Audio CODEC (ALC655)



# KBC


Internal Keyboard Connector
FPC/FFC/1MM/26P
ACES
85202-26-00
291000152603
30mil
120Z/100M 1608
W83L950D
PQFP80_0.5MM
2.5V LEVEL
For KBC Reset
Threshold : 2.93V
Thermal Protection
I2C / SMB Address : 98h
R01
R0A
DF13-3P-1.25V
291000010303
DTC144WK
DTC144TKA
MLL34B
RLS4148
AO3409
SOT23_FET
SOT23AN_1
IMP811
SOT143
286300811001
LM86
SO8
284500086001
TC010-PSS11CET
297140200001
ESD0805A/NA
8MHZ
TXC8X4.5
MITAC
KBC (W83L950D)
316685200002
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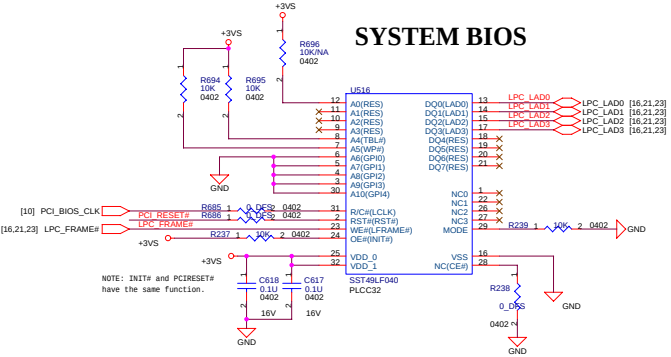
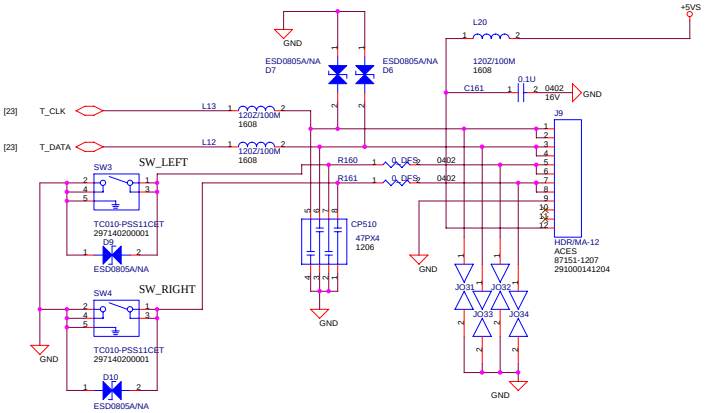
# BIOS / TouchPad / Through Hole

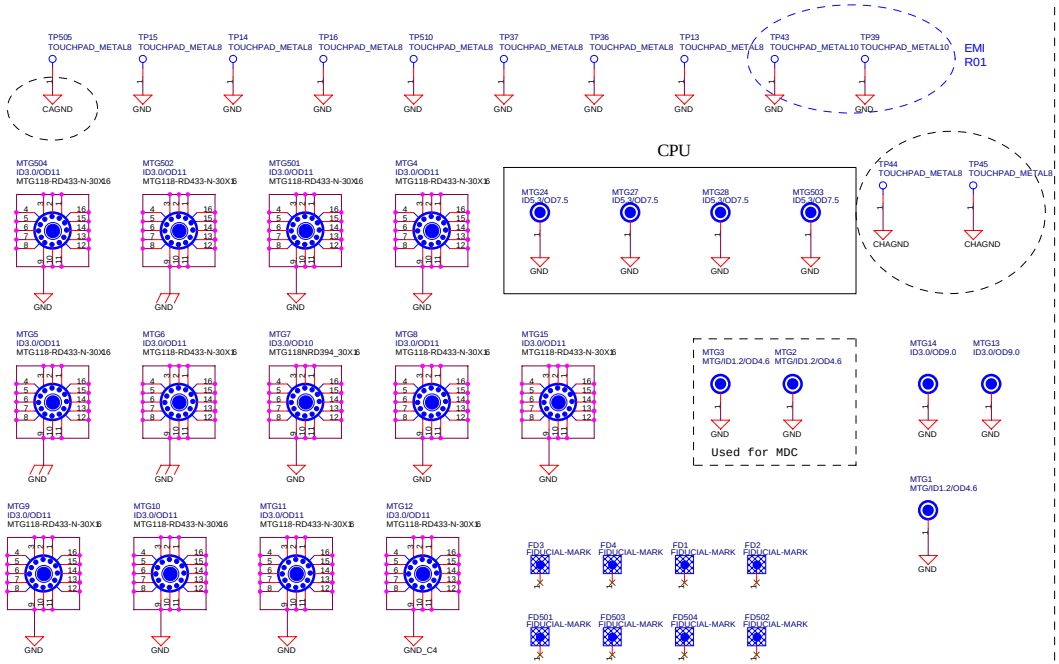
## SYSTEM BIOS



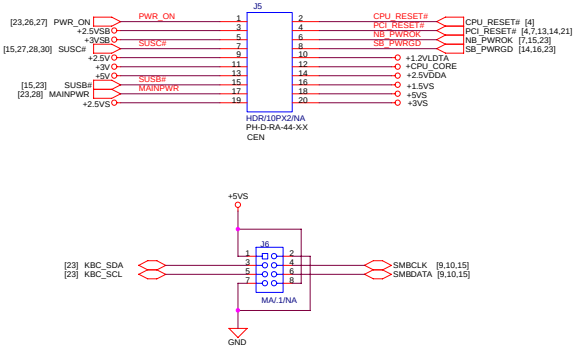

## TOUCH PAD




## CPU




**For debug only (6 mil)**




| | | | |
|---|---|---|---|
| Title | BIOS / TP / HOLE | | |
| Size | Document Number | 316685200002 | Rev R02 |
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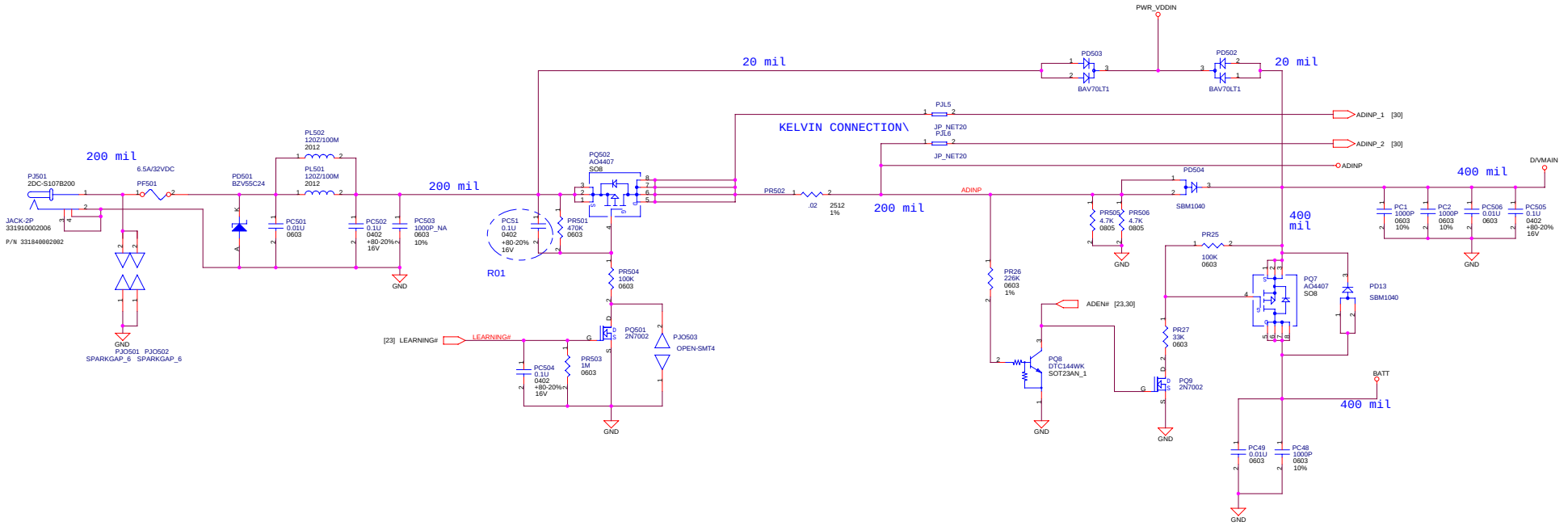
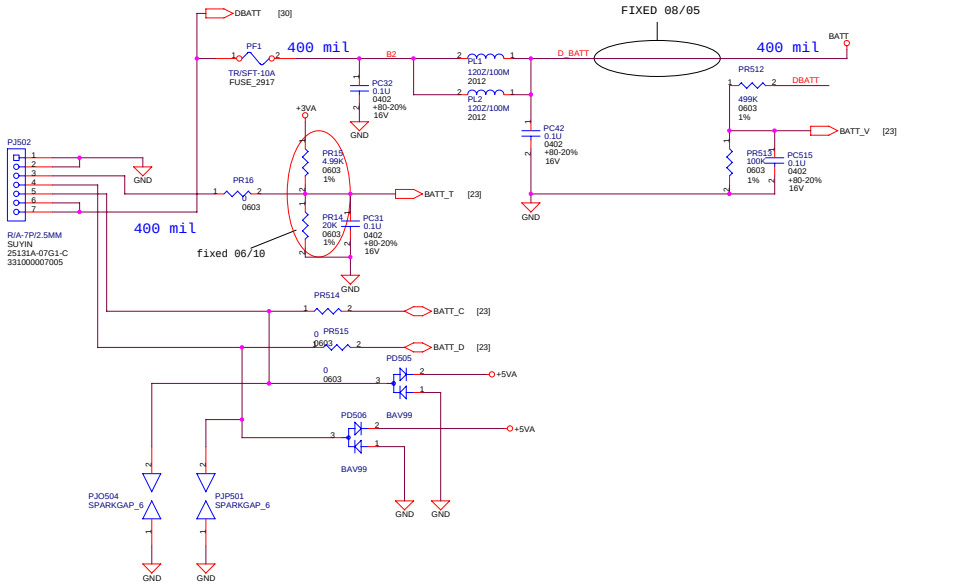
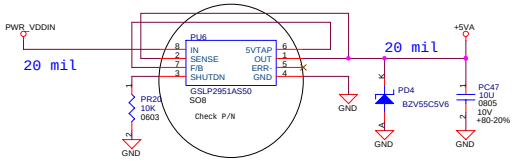
# ADP IN / BATT IN / +5VA / +5VAS

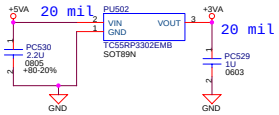



## +5VA

## RTC BATTERY




| | |
|---|---|
| MiTAC | |
| Title | ADP IN & BATT IN |
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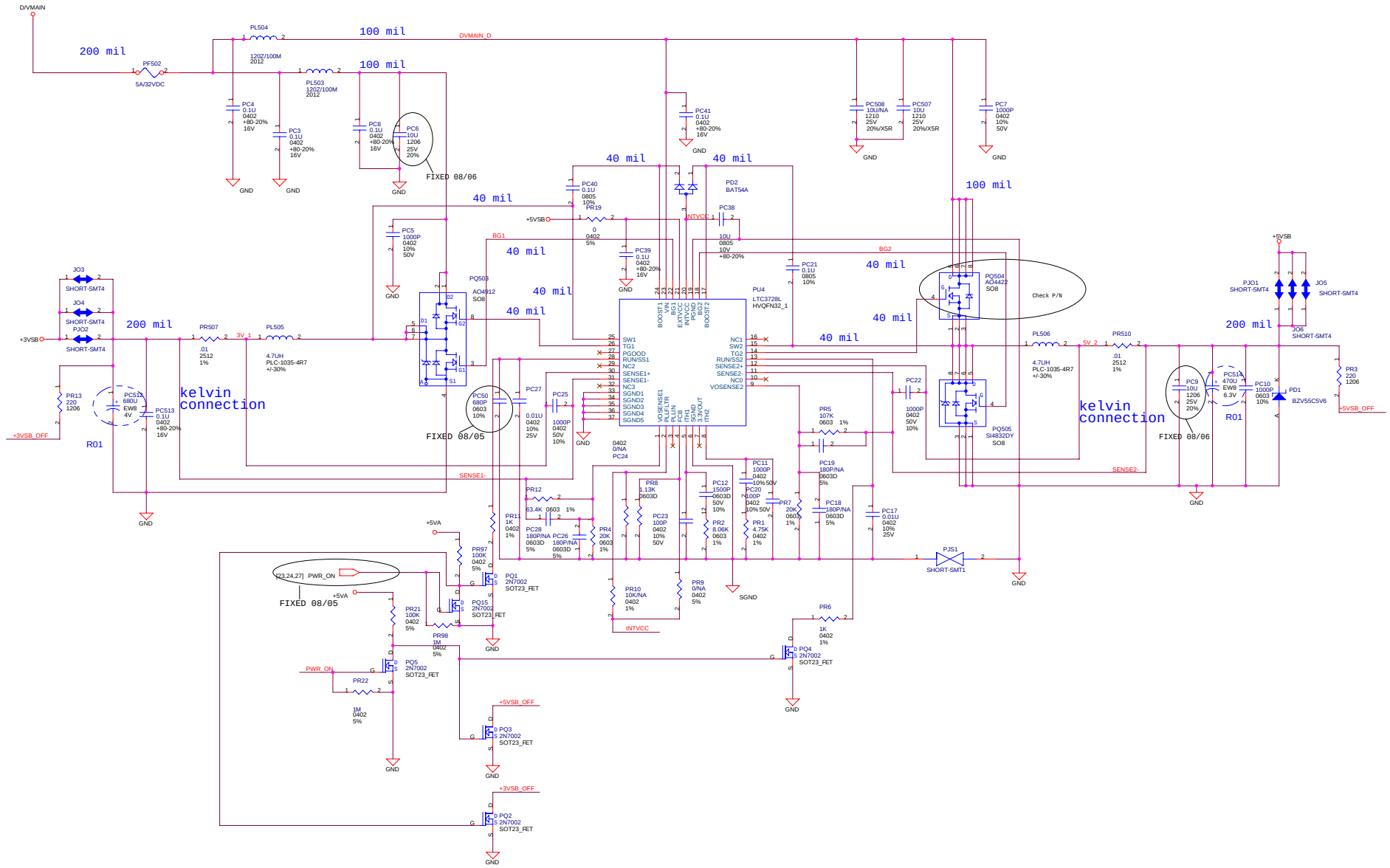


MiTAC

| | | |
|---|---|---|
| Title | +5V,+3V | |
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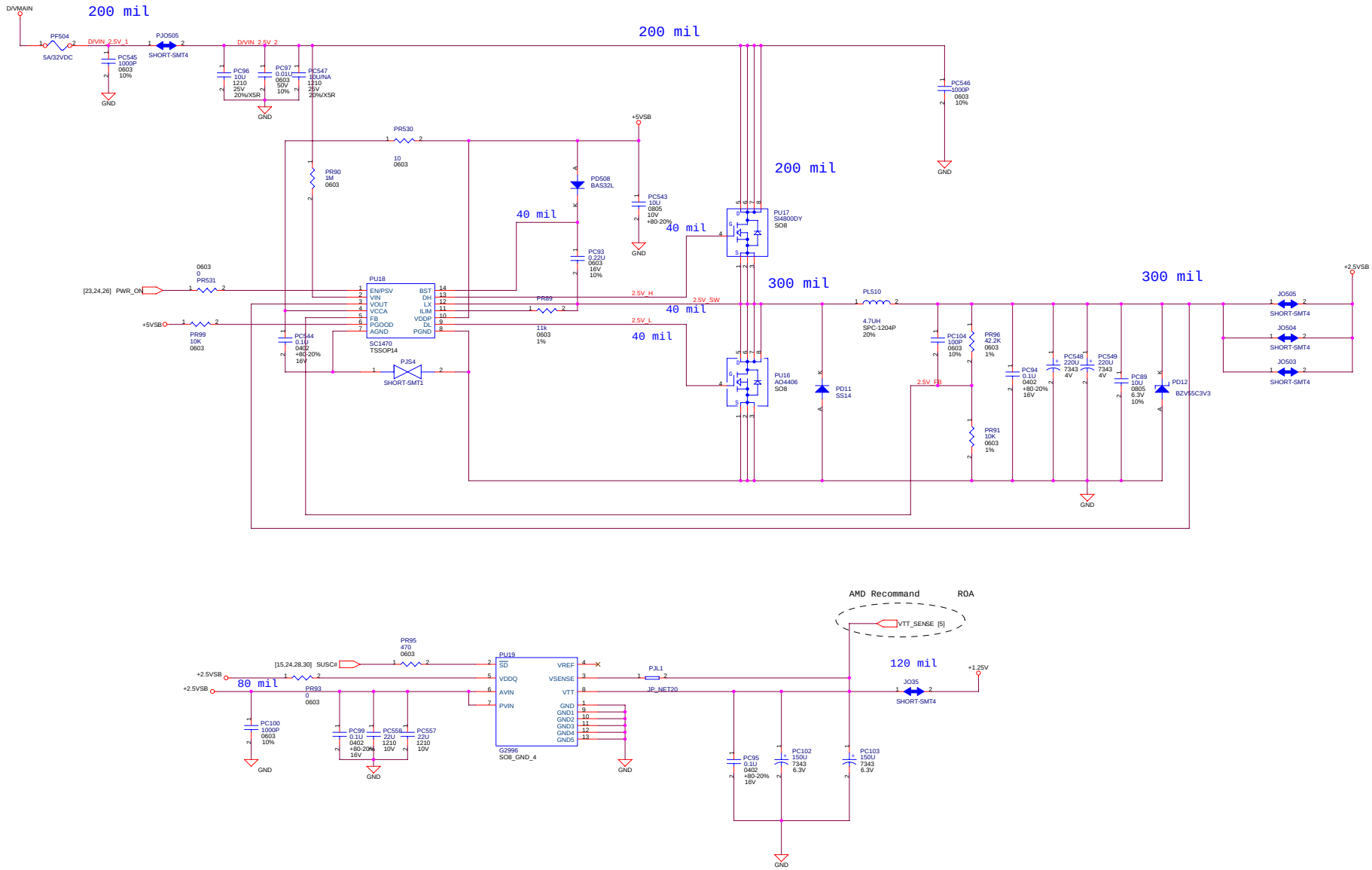


MiTAC

| | | |
|---|---|---|
| Title | +2.5V,+1.25VS | |
| Size: Custom | Document Number: 316684700001 | Rev: R02 |
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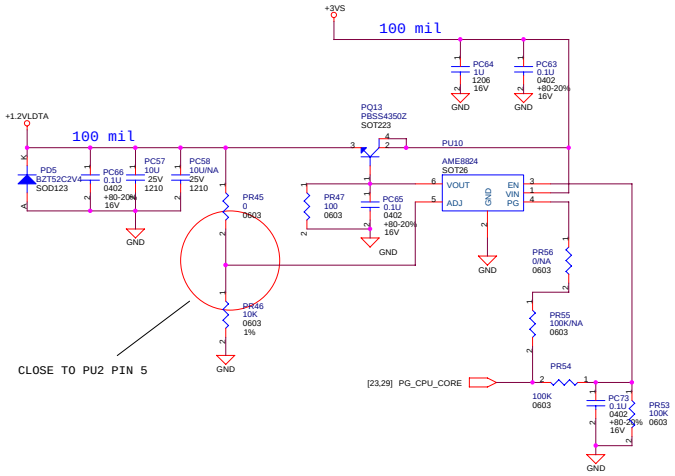
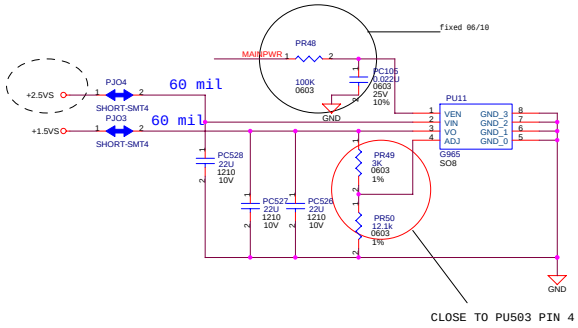
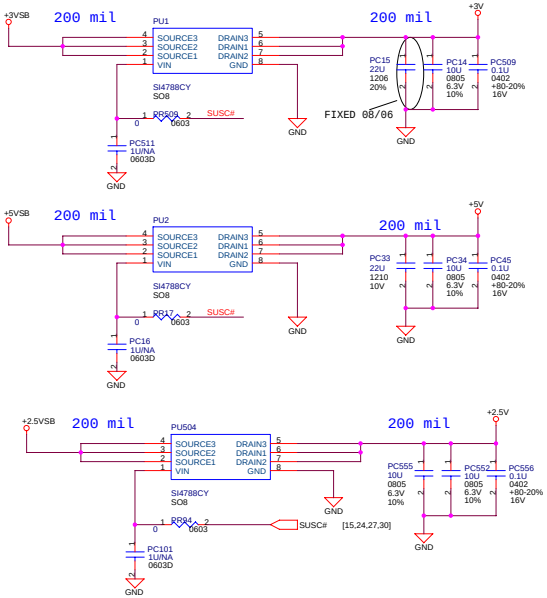
## +1.2VLDTA



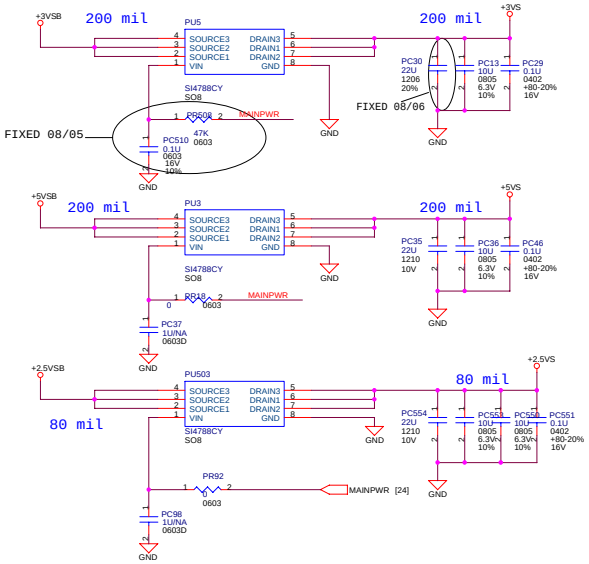

## +1.5VS



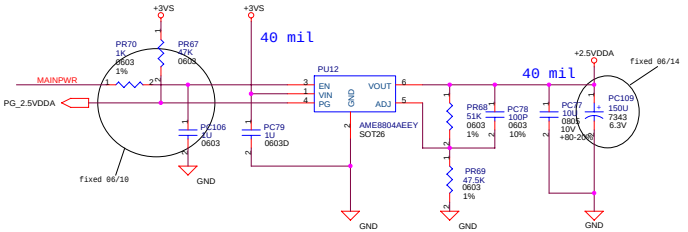

## 3V / 2.5V




## 3VS / 5VS / 2.5VS




## 2.5VDDA





MiTAC

Title: +5VS,+3VS,+2.5VS,+1.5VS,+2.5VDDA,+1.2VLDTA

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**For low power CPU , voltage offset -100mV-----a**
**Transient : +100mV to -50mV; Offset will be +50mV------b**
**a,b--->Total offset will be -50mV(Without pin 5 OFS offset)**

**Ros = RFB*(5V-VID)/Vos**
**PR61= PR76*(5V-VID)/50mV**
**If VID 1.35V**
**PR61=3.6K*(5V-1.35V)/100mV=131.4K**

| GPIO | +CPU_CORE |
|---|---|
| 1 | 1.35V |
| 0 | 1.25V |

**Vdroop=Idroop*PR17 ~ Isen*PR17 ~ 72.6mV**
**If PR59 NA, Vdroop=0**

**ROFS = VOFS*10/100uA**
**PR62=32.4mV*10/100uA = 3.24K**
**PR79 : 107K Ohms -----> f ~ 250K HZ**

**Over current trip level : 90uA(typ.)**
**Full load Isen current : 90uA/1.5 ~ 60uA**
**Rds(on) * Io = Rsen * Isen**
**6.5m*1.5*15A*1.5 = Rsen*60uA**
**Rsen = 3.65K**
**OCP :15A*1.5*2 = 45A**

AMD spec.:
Output Cap.4800uF
Actually output cap.:4690uF

| | |
|---|---|
| Title | +CPU_CORE |
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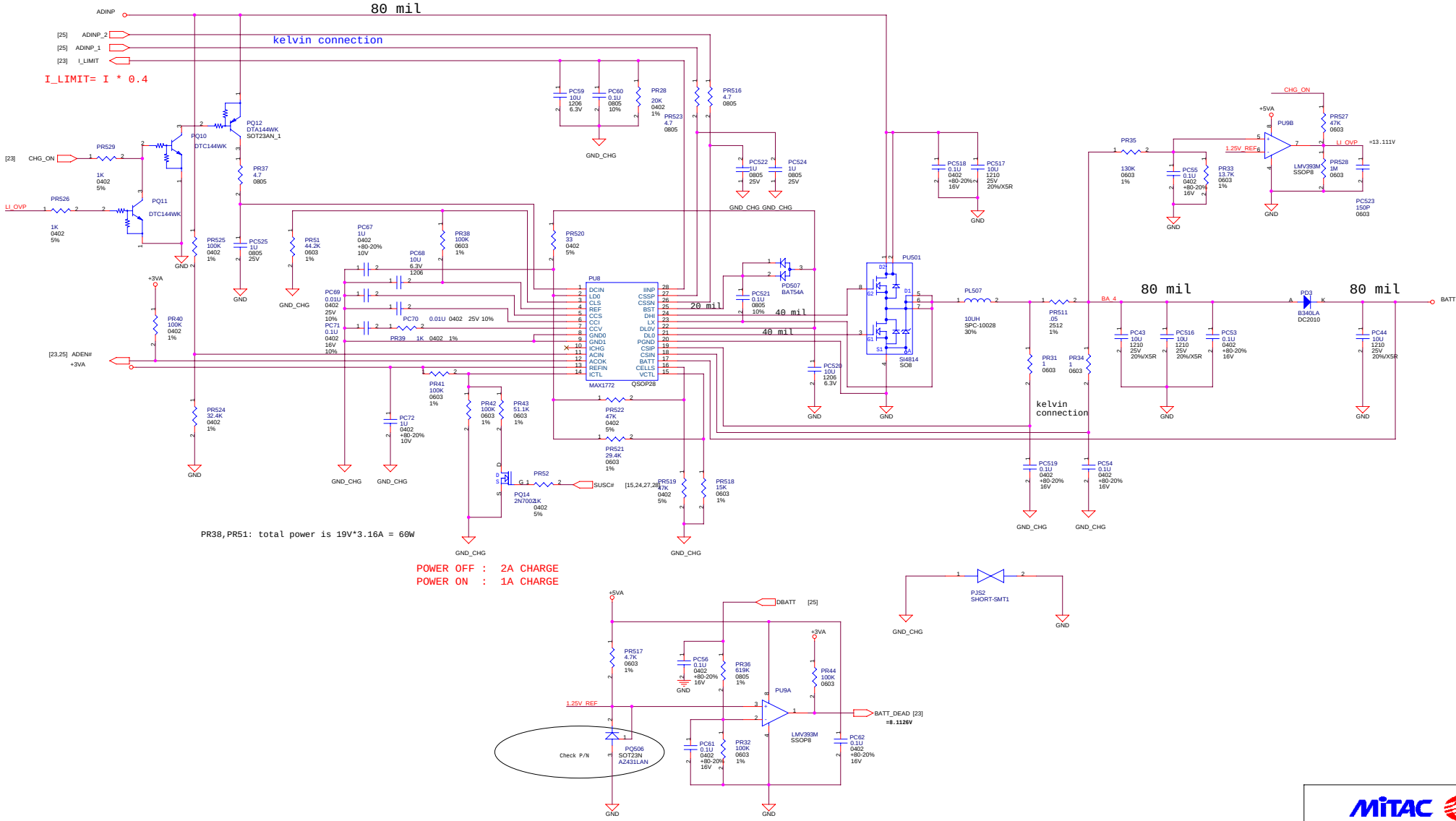
# CHARGING




| | | | |
|---|---|---|---|
| Title | Charger | | |
| Size: Custom | Document Number: 316684700001 | | Rev: R02 |
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## Reference Material

| | |
|---|---|
| ❖ Mobile AMD Athon64 Processor Data Sheet | AMD.INC |
| ❖ VIA K8N800 North Bridge | VIA.INC |
| ❖ VIA VT8235 CE South Bridge | VIA.INC |
| ❖ Clock Generator ICS950405 | ICS.INC |
| ❖ Keyboard controller W83L950D Data Sheet | WIN.INC |
| ❖ 8889 Hardware Engineering Specification | Technology.Corp./MiTAC |

# SERVICE MANUAL FOR 8889

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Author : Star Meng

Assistant Editor : Ping Xie

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